AIP | Applied Physics Letters

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Citation: Appl. Phys. Lett. **96**, 013507 (2010); doi: 10.1063/1.3284650
View online: http://dx.doi.org/10.1063/1.3284650
View Table of Contents: http://apl.aip.org/resource/1/APPLAB/v96/i1
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Efficient heterojunction solar cells on *p*-type crystal silicon wafers

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(Received 2 October 2009; accepted 14 December 2009; published online 6 January 2010)

Efficient crystalline silicon heterojunction solar cells are fabricated on *p*-type wafers using amorphous silicon emitter and back contact layers. The independently confirmed AM1.5 conversion efficiencies are 19.3% on a float-zone wafer and 18.8% on a Czochralski wafer; conversion efficiencies show no significant light-induced degradation. The best open-circuit voltage is above 700 mV. Surface cleaning and passivation play important roles in heterojunction solar cell performance. © *2010 American Institute of Physics*. [doi:10.1063/1.3284650]

Crystalline silicon (c-Si) heterojunction (HJ) solar cells are under intense investigation worldwide[1–7] following pioneering efforts at Sanyo Corporation. Si HJ cells have many advantages over conventional diffused-junction Si cells, including (1) lower temperature (<250 °C) processing, (2) higher efficiency, (3) higher open circuit voltage, and (4) a lower temperature coefficient describing the reduction of performance with increasing temperature. High performance commercial Si HJ cells are all made from *n*-type wafers. The best reported AM1.5 efficiency is 23%.[1] The best reported open circuit voltage is 739 mV.[6] While *n*-type silicon wafer appears to be an excellent base material for high efficiency (>20%) modules with high annual energy output, development of viable *p*-wafer cells would open many industrial PV options. In this letter, we report solar cells with 19.3% energy conversion efficiency on *p*-type float-zone (FZ) Si wafers and 18.3% on *p*-type Czockralski (CZ) Si wafers. Our best open-circuit voltage is higher 700 mV. We find that there is little degradation of our Si HJ solar cells on CZ *p*-type c-Si under prolonged light exposure. Despite the higher *n*-type Si efficiency, it could be advantageous to make Si HJ modules on widely available boron-doped Si wafers.

Si heterojunciton solar cells use thin hydrogenated amorphous silicon (a-Si:H) as a wide band gap layer on both sides of a high quality c-Si wafer that effectively passivates both a front heterojunction emitter that collects minority carriers and a back contact that collects majority-carriers.[8] A schematic equilibrium energy diagram of a *p*-type c-Si heterojunction cell with a-Si:H contacts is shown in Fig. 1. The values of band gap for various thin layers are based upon optical measurements. We use 1.75 eV for a-Si:H, P-, B-, and intrinsic layers and 3.70 eV for indium tin oxide (ITO). The Fermi level of ITO is slightly above its conduction band (0.1 eV). Band gap of bulk c-Si is 1.14 eV. In general, the contacts between ITO and the doped layers behave as Ohmic contact. We also include the conduction band offset (ΔE_c) and valence band offset (ΔE_v). The exact values of those offsets are difficulty to measure. The early reported photoemission values were 0.1 eV for ΔE_c and 0.4 eV for ΔE_v,[9] and recent measurements have generally agreed well. At the emitter side, the low ΔE_c allows electrons to move into the a-Si:H *n*-layer and the high ΔE_v blocks holes at the interface. The a-Si:H heterojunction at the front is nearly ideal for electron collection. At the back contact, there is a low ΔE_c and high ΔE_v. The high valence band offset might be expected to prevent holes from moving freely to the a-Si:H *p*-layer. However, holes do pass through the barrier at the a-Si:H *p*-layer by tunneling, hopping, or thermally assisted tunneling. From Fig. 1, it is clear that an *i*/*p*-layer with high ΔE_c and low ΔE_v would improve hole collection. Modeling by Kanevce and Metzger.[10] suggests that high majority carrier density of holes in *p*-wafer Si HJ cells has the advantage of avoiding the high barrier for minority carrier hole collection at the *p*-type emitter in *n*-type Si HJ solar cells.

We use high quality FZ *p*-type crystal Si wafers and CZ wafers for high-efficiency cell development and scientific studies. The Si wafers are (100) orientated, 220–300 μm thick, and 1–4 Ω cm in resistivity. The minority carrier lifetime for surface-passivated wafers is on the order of 1 ms, as measured by a Sinton PCD lifetime tester.[11] We use 2%–5% KOH with IPA at 80 °C to texture *p*-type wafers. The feature size of the pyramids is less than 10 μm.

The cell structure is metal grid/ITO/*n*/*i*/c-Si(*p*)/*i*/*p*/ITO/metal and metal grid/ITO/*n*/*i*/c-Si(*p*)/*i*/*p*/metal. The c-Si wafer size is about 2.5×4.5 cm^2. The thicknesses of the *n*/*i* layer and *i*/*p* a-Si:H layers are about 10 nm with *i*-layer at 4 nm deposited by the hot wire chemical vapor

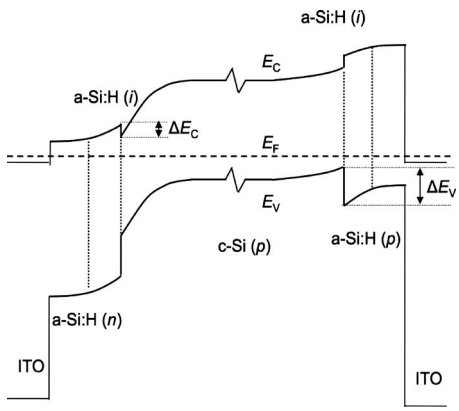

FIG. 1. A schematics of energy diagram of a double-sided a-Si:H/c-Si heterojunction solar cell at equilibrium condition. Top solid lines are conduction band (E_c), and bottom solid lines are valence band (E_v). The dashed lines are Fermi energy (E_F). ΔE_c and ΔE_v are band offsets at conduction and valence bands, respectively.

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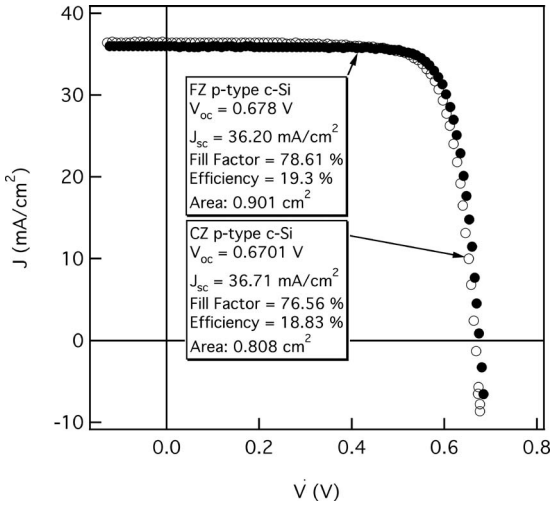

FIG. 2. Solar cell performance of our best silicon heterojunction on *p*-type c-Si. Solid circle symbol is for FZ Si wafer and open circle symbol is for CZ Si wafer.

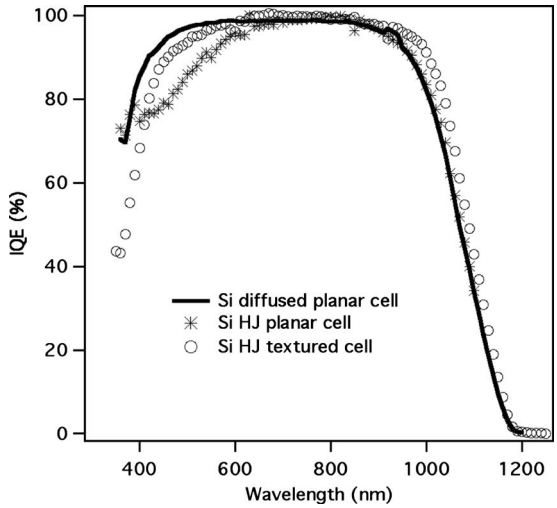

FIG. 3. Internal quantum efficiency comparison among standard diffused cell (solid line), planar heterojunction cell (cross symbols), and textured double-side heterojunction cell (open circle symbols).

deposition technique. The total thickness of n/i layer or i/p a-Si:H layers is confirmed by tunneling electron microscope measurement. The thicknesses of front ITO are about 760 nm and 900 Å for planar and textured wafers, respectively. We make two 1 cm^2 cells or one 4 cm^2 cell per sample and it is defined by the area of ITO. Detail of cell process is published elsewhere.[3] An aperture mask is used during the cell current-density voltage (J/V) measurement. Confirming J/V measurements are made at NREL by the accredited PV Performance Characterization Team.

Figure 2 shows confirmed J/V curves of cells on *p*-type FZ and CZ Si wafers. The 19.3% Si HJ cell on *p*-type FZ wafer has a V_{oc} of 678 mV, fill factor (FF) of 0.786, and short-circuit current density (J_{sc}) of 36.2 mA/cm^2. The cell aperture area is 0.901 cm^2. Our best unconfirmed open circuit voltage is 701 mV on a 4 cm^2 cell. The 18.8% Si HJ cell on *p*-type CZ wafer has a V_{oc} of 670 mV, FF of 0.765, and J_{sc} of 36.71 mA/cm^2. The cell aperture area is 0.808 cm^2. We also performed light soaking experiment on both FZ and CZ *p*-type Si HJ solar cells. Our data show that the solar cell performance was quite stable under AM 1.5 light illumination up to 1000 h. The cell efficiency falls 2.6% for the FZ cell and 1.3% for the CZ cell. These changes are within our measurement error of ±4% and not likely connected to a-Si:H related light induced degradation, which is about 20%–30% using much thicker a-Si:H in the cells.

Careful Si wafer surface preparation is essential because impurity energy levels in the gap can cause interface recombination that reduces V_{oc} and efficiency. We successively developed four generations of improved cleaning procedures for planar Si wafers[12] and improve the V_{oc} from 630 mV to just over 700 mV. In Generation 1, we reached 630 mV by boiling the wafer in 18 MW cm high-purity deionized (DI) water rinse, followed by a long DI water rinse, and a 0.5% HF treatment until the surface became hydrophobic due to oxide removal. This procedure gave us V_{oc} of 630 mV. In Generation 2, we increased V_{oc} to 680 mV by adding more chemical modification of the surface, including oxidation followed by HF stripping and more aggressive acid cleaning solution. In Generation 3, we reached 690 mV by alternating the aggressive acid cleaning of generation 2 with a long DI water rinse. In Generation 4, we increased V_{oc} to 701 mV by better controlling contamination from the organic degreasing step and increasing the purity of chemicals that we used for the final chemical oxidation step. During this time, there were also improvements made to a-Si:H deposition conditions, but surface cleaning remains a key component of cell efficiency. To clean our best textured wafer cells, however, we use a standard Radio Corporation of America 1 and 2 cleaning procedure. Although this cleaning does not produce the best V_{oc} it can remove residual impurities to give us our best efficiencies. In our work on textured wafers, we found that the Generation 4 cleaning procedure removed some of the sharp textured features. We could obtain high V_{oc} with this procedure but lost some of the optical enhancement that texturing provides.

We made a sequence of changes to a baseline diffused-junction *p*-wafer cell to better understand what factors control V_{oc} in Si HJ cells. The diffused junction cell on planar *p*-type wafer cell had a V_{oc} of 630 mV. Our front-only single heterojunction Si HJ cell with a similar Al/BSF gave a V_{oc} of 652 mV after we optimized the thin a-Si:H emitter layers to achieve a very low surface recombination velocity (SRV) of 15 cm/sec. For comparison, a typical Al/BSF Si wafer has a back surface-recombination velocity (BSRV) of ~1000 cm/sec. Further improvements led to a V_{oc} of 700 mV on *p*-type planar silicon wafers. When we omit the *i*-layer from the front heterojunction emitter, the V_{oc} is only about 600 mV. To achieve high V_{oc} and efficiency, the c-Si surface needs to be well passivated by an intrinsic a-Si:H layer. Avoiding formation of epitaxial c-Si or nanocrystalline Si (Refs. 3 and 13) is critical for the passivation, most likely because of the low structural quality of epitaxial Si formed at 100 to 300 °C.

In order to improve the cell's short-circuit current density, wafer was textured with random pyramids. Our best J_{sc} increases from 32 mA/cm^2 for a planar cell to 36.7 mA/cm^2 in a textured cell. The V_{oc} of 678 mV in the textured cell is not as high as we can achieve on a planar surface, likely because of difficulties in cleaning the textured surface, especially where the pyramid bases meet.

Figure 3 shows internal quantum efficiency (IQE) data

from three cells: a standard diffused-emitter planar cell with Al/BSF, a front only Si HJ planar cell with Al/BSF, and a double-side HJ textured cell. The Si HJ cell shows poor response in the blue compared to the diffused-emitter cell. The front-only HJ cell provides 1.27 mA/cm^2 less J_{sc} than the diffused cell from 350 to 700 nm (integration of IQE against AM1.5 spectrum). This loss is due to absorption of incident light in the front ITO and a-Si:H layers. The textured double-side Si HJ cell provides only 0.60 mA/cm^2 less current than the diffused junction cell from 350 to 700 nm. The 0.67 mA/cm^2 gain in J_{sc} is results in multiple light scattering at the pyramids surfaces. Textured cell also eliminates the Al/BSF contact to produce far better infrared response from 900 to 1200 nm.

Other advantage of the Si HJ cells is that it can enable the continuing reduction in wafer thickness required for a cost-effective Si PV industry. As cells become thinner, low-recombination surfaces become progressively more important.[14] To obtain a V_{oc} over 680 mV, we find that a 200 μm *p*-type wafer must have a minority carrier lifetime over 700 μs after a-Si:H heterojuncton emitter and back contact are applied. This enables the solar cells to have a minority carrier diffusion length much larger than its thickness. However, the requirement for high bulk lifetime will be relaxed in wafers thinner than 100 μm. Because of the square root dependence of diffusion length on lifetime, when the thickness of the Si wafer is reduced by half, the bulk lifetime can be reduced by four times. Based upon our high performance cell with lifetime of 700 μs on 200 μm wafer, it suggests a 100 μm *p*-wafer cell can tolerate a 200 μs lifetime. However, careful preparation, cleanliness, and control of the critical front and back surface heterointerfaces will be necessary for future thin c-Si heterojunction solar cells.

The authors thank R. Crandall, D. Young, C. Teplin, and S. Ward for discussion and assistance with processing and measurements. Authors are also indebted to Dr. Ajeet Rohatgi and Dr. Vijay Yelundur at Georgia Institute of Technology. This work was supported by the U.S. Department of Energy under Contract No. DE-AC36-08-GO28308.

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