

A Dissertation
entitled
Electro-structural coupling in chalcogenide thin film devices:
photovoltaics and phase change memory

by
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As partial fulfillment of the requirements for the
Doctor of Philosophy Degree in Physics

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College of Graduate Studies

The University of Toledo
May, 2008

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An Abstract of

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This work is primarily a study of electro structural coupling in thin film chalcogenide devices and its applications to Photovoltaics (PV) and phase change memory (PCM); which both utilize the same class of materials, called the chalcogenides.

We have studied the piezo- and pyro-electricity in CdS based photovoltaics including CdTe and CuIn(Ga)Se₂ based devices, using three experimental setups to provide squeezing, bending and flexing deformations. We show that the pyro- PV coupling is an important factor changing the electric field distribution and strongly affecting the device parameters like working voltage, short circuit current, field factor and efficiency. New technological implications are discussed.

Structural transformations were also studied in chalcogenide based phase change memory devices. The phenomena of PCM switching and temporal drift of parameters of PCM have been experimentally studied in great detail and verified with a theoretical model. The time dependent behavior of PCM nano glasses was tracked in time. Our data on the drift dynamics of PCM parameters are explained based on the

classical double well potential concept of structural relaxations as a universal glass dynamics. Our findings show for the first time that the threshold voltage V_{th} and the amorphous state resistance R drift as $\Delta V_{th} \propto \ln t$ and $R \propto t^\alpha$, where t is the time.

As another step in exploring the switching phenomena in chalcogenide glasses, we have studied the underlying science of field induced nucleation and have found that the field induced nucleation takes place in phase change memory. We present experimental data on switching in phase change memory for times and temperatures significantly different from the typical reported values. We have for the first time observed a new phenomenon of the under-threshold switching at room temperature. A theoretical model was outlined with an understanding that nucleation of cylinder shaped crystal particles with barriers significantly lower than that of spherical nuclei and an analytical expression for minimum threshold voltage was predicted below which the switching concept fails. Our experimental results agree well with the theory.

Acknowledgments

I am profoundly grateful to my Academic Advisor, Dr. Victor G. Karpov, for his immense help, guidance and encouragement. His motivations in studying the physics of electronic devices has been an ample source of inspiration for me.

I am also indebted to my Ph.D. advisory committee Drs. Sanjay Khare, Daniel Georgiev, Jon Bjorkman and Brian Bagley for their support, advise and valuable suggestions.

I would express my gratitude to the photovoltaic group and the department of physics and Astronomy at the university of Toledo for equipping me with knowledge and skills essential for achieving this honorable degree. Financial support from the department of physics and Astronomy, University of Toledo is acknowledged with pleasure.

It is my pleasure to acknowledge the help of my former advisor and committee member Dr. Ale Lukaszew, now a professor at College of William & Mary.

My sincere thanks to Intel corporation, phase change memory division at Santa Clara, CA and specially to my manager Dr. I. V. Karpov (Intel Corp.) for giving me a financial support and opportunity to work as a Graduate Intern and guiding my research on Phase change memory for almost a year. Special acknowledgement to senior engineer Andrew Gordon (Ovonyx Inc.) and Technician Jaime Rivera (Ovonyx Inc.) for helping me in carrying out those PCM experiments at Intel corporation.

My Special thanks to the members of our group led by Dr. Victor Karpov, including Drs. Diana Shvydka and Jennifer Drayton, who taught me particularly the experimental techniques in photovoltaics. I thank other group members Yevgen Kryukov, Lilani Cooray, Marco Nardone, Tim Muszyaski, and Trevor Wilson for helping me through multiple fruitful discussions and critiques, both individually and during our group "tea seminar series" where physics was always talked informally and friendly.

Last but not the least my parents back in India, my sister, her husband and finally my fiancee Rakhi and her family for supporting me to complete my PhD degree.

Contents

Abstract	ii
Acknowledgments	iv
Contents	v
List of Figures	viii
List of Tables	xviii
1 Introduction	1
1.1 Chalcogenide Materials and their use in PV and PCM	3
1.2 Piezo and Pyro coupling in chalcogenide thin film photovoltaics	4
1.3 Phase change Memory Structural Transformations Amorphous- Crystalline	5
2 Piezo & Pyro Photovoltaic Coupling	7
2.1 Introduction	7
2.2 Physical aspects of piezo-photovoltaics	11
2.2.1 Characteristic parameters	11

2.2.2	Internal screening	15
2.2.3	External screening	18
2.3	Experimental	29
2.3.1	Piezo-effect setups	29
2.3.2	Piezo-data	36
2.3.3	Other related experiments	42
2.4	Device operations & Model	44
2.5	Discussion	46
2.6	Conclusions	50
3	Fundamental drift of Parameters in Phase Change Memory	51
3.1	Introduction	51
3.2	Experimental	54
3.3	Phenomenological DWP model	59
3.4	Discussion	69
3.5	Conclusions	70
4	Field Induced Nucleation in Phase Change Memory	71
4.1	Introduction	71
4.2	Model	72
4.3	Experimental	76
4.4	Thermal Analysis	82
4.5	Conclusions	85

5	Conclusions	86
A	Piezo & Pyro Photovoltaic Coupling	87
A.1	Device operations and Model	87
B	Model of field Induced Nucleation in Phase Change Memory	92

List of Figures

2-1	Sketch of CdTe/CdS PV cell (a) and CuIn(Ga)Se ₂ PV cell (b) corresponding to the superstrate and substrate structure respectively; TCO stands for the transparent conductive oxide. Arrows show the direction of incident light.	8
2-2	(a) Piezoelectric element of the hexagonal CdS structure showing predominantly Cd and predominantly S terminated planes. (b) Direction of forces affecting the piezoelectric element. Directions X, Y, or Z are represented by the subscript 1, 2, or 3, respectively. Shears about these axes are represented by the subscripts 4,5, or 6 respectively.	12
2-3	Sketch of the mechanisms of piezo-electric polarization along Z axis in response to the stress (shown by arrows) parallel to Z axis (d_{33} effect) and to X axis (d_{31} effect).	13
2-4	Screening of the piezo- and pyro-electric fields in CdS in the cases of strongly doped (a) and intrinsic (b) uniform materials.	16

2-5	(a) Sketch of CdS grain composed of many randomly oriented nanocrystals; arrows showing their electric polarizations. (b) Top: randomly polarized grains forming a film with zero average polarization. Bottom: Grain alignment in the external electric field leading to a film with finite polarization	19
2-6	(a) Sketch of electric charge distributions in a structure of metal-pyroelectric film-semiconductor for the case when the screening (depletion) length in semiconductor is much greater than the film thickness l . The metal polarization charge is not shown. \mathbf{P} is the vector of polarization. (b) The same for the opposite limiting case $l \ll L$. (c) The equilibrium electron potential energy for the case (b). ϕ_F is the Fermi potential.	20
2-7	(a) The electric charge distribution in a structure of metal - pyroelectric film - semiconductor; the metal polarization is not shown. (b) The electron potential energy for the case when there is no pyroelectric film (dashed line) and for the case when the film is present. Not to scale: $l/L \ll 1$	23
2-8	(a) The dipole layer and its electric field lines having components parallel to the metal surface. (b) The dipole layer and its image charge generate the electric field, which lines are perpendicular to the surface.	27

2-9	Sketch of apparatus used in our squeezing experiments for applying pressure perpendicular to the face of thin-film PV cell. LS1 (under the cell stage through the fiber optics) and LS2 show the two positions of light source used respectively in the cases of superstrate and substrate cell configurations.	29
2-10	Sketch of apparatus used in our bending experiments with glass superstrates for applying stress parallel to the face of thin-film PV cell. R-labelled circles stand for the cylindrical metal rods perpendicular to the plane of the diagram. LS denotes the light source.	30
2-11	(a) Sketch of apparatus used in our flexing experiments for applying stress parallel to the face of thin-film PV cells made on flexible substrate. LS denotes the light source. (b) Geometrical dimensions of flexing experiment; y is the arrow of bending.	31
2-12	Pressure induced evolution of the current voltage characteristics of CdTe cells in squeezing experiments.	36
2-13	Open circuit voltage (V_{oc}) and short circuit current (J_{SC}) of the CdTe/CdS solar cell versus pressure. Arrows show the directions of pressure change.	37
2-14	Short circuit (R_{sc}) and open-circuit (R_s) resistance vs. device V_{oc} driven by the external pressure. The dependencies include both the pressure up and down sweep data points showing almost no hysteresis in this format. The curve shows a fit of R_{sc} by Eq. (2.25) where R_s is given by the data.	38

2-15	Open circuit voltage (V_{OC}) and short circuit current (J_{SC}) of the CdTe/CdS solar cell versus pressure. Arrows show the directions of pressure change.	39
2-16	Open circuit voltage (V_{OC}) and short circuit current (J_{SC}) of the CIGS solar cell versus pressure. Arrows show the directions of pressure change.	39
2-17	(a) Pressure induced evolution of the current voltage characteristics of CdTe cells in bending experiments. (b) Open circuit voltage (V_{OC}) and short circuit current (J_{SC}) of the CdTe/CdS solar cell versus pressure in bending experiments. Arrows show the directions of pressure change.	40
2-18	Stress-induced evolution of current-voltage characteristics of CdTe cells on flexible substrates.	41
2-19	Stress-induced evolution of open-circuit voltage (V_{oc}) and short-circuit current (J_{sc}) of CdTe cells on flexible substrates under different light intensities.	42
2-20	X-ray diffraction spectra of CdS/CdTe solar cell deposited on TCO for three different CdS layer thicknesses.	43
2-21	Design of the experiment for CdCl ₂ treatment of CdTe cells under external electric bias.	44

2-22	Open circuit voltage (V_{oc}), short circuit current (J_{sc}), fill factor (FF), and efficiency (Eff) vs. polarization electric field strength \mathbf{E} . Positive field region corresponds to the case of polarization shown in Fig 2-6, Fig 2-7 , called 'gull- wing model [59]. The dashed branch of the V_{oc} curve corresponds the shunting current cutoff beyond the AMPS modeling capabilities.	45
3-1	(a): Atomic arrangement of metastable $\text{Ge}_2\text{Sb}_2\text{Te}_5$ built based on (111) planes along the [111] direction. (b): Stable crystal structure of hexagonal $\text{Ge}_2\text{Sb}_2\text{Te}_5$	52
3-2	The typical PCM current-voltage (IV) characteristics include domains corresponding to: 1 - conductive phase, 2 - insulating phase, 3 - switching, 4 - post-switching. Shown on the inset is a sketch of the experimental setup. V_A and $V_P = V$ are respectively the applied and the probe measured voltages, whose differential determines the current (I) as divided by the load resistance (R_L).	53
3-3	definition of the drift time t . The read voltage much lower than V_{th} allows measurements without causing any structural changes.	54
3-4	Basic Block diagram of the measurement circuit used to measure the Drift of $V_{th}(t)$ and R . General Purpose Interface Bus (GPIB), Digital Analog Converter (DAC) and Oscilloscope (OSC) were used in the circuit.	55

3-5	Drift $V_{th}(t)$ pulse measurement technique for different partially reset PCM cells.	56
3-6	Drift $V_{th}(t)$ for three partially reset PCM cells, in which the amorphous region was created under different reset voltages shown next to the curves. The inset PCM sketch [64] shows the crystalline and amorphous (A) GST phases, the small area electrode (SAE) and thermal insulator (TI).	57
3-7	Drift $V_{th}(t)$ for three partially reset PCM cells, same as in Fig. 3-6, normalized to the absolute values of the corresponding voltages at 0.1 ms.	58
3-8	Temporal drift of $V_{th}(t)$ and $R(t)$ arbitrarily normalized to $t = 0.1$ ms and $t = 2$ s respectively. Note the logarithmic scale of the R -axis. . .	59
3-9	Drift of threshold voltage $V_{th}(t)$ normalized to the the corresponding initial values for fully reset samples of different thicknesses between 150Å and 1000Å.	60
3-10	Drift coefficient of threshold voltage $V_{th}(t)$ vs.various Thickness of GST.Note that there is a 15 %-20 % variation in drift coefficient which can be due to experimental inaccuracy.	61
3-11	Drift $V_{th}(t)$ and $R(t)$ at two temperatures.	62
3-12	Pulse Measurement Technique for measuring Drift of $V_{th}(t)$ and $R(t)$ of PCM cells at two temperatures.	62
3-13	Threshold voltage $V_{th}(t)$ for fully reset samples of different thicknesses of 300Å, 500Å and 700Å.	63

3-14	IV characteristics of a typical GST material measured at Intel Lab showing that higher thickness of GST has higher threshold voltage. In this case 1000Å has V_{th} of 1.5v and 150Å has V_{th} of 1v.	64
3-15	Double well atomic potential (DWP) with the barrier height W_B . . .	65
3-16	Saturation of $V_{th}(t)$ after high temperature anneal vs. lack of saturation at room temperature. All the data were read at 25 C.	66
3-17	Saturation behavior of R at 75c compared to no saturation behavior of R at 25c.	67
3-18	Experimental set up to study the saturation behavior of V_{th} (anneal time) and R (anneal time). The PCM devices (sample) were initially heated in the chuck to the desired temperature of 75c or 100c for those annealed times, mentioned in the plot. Then they were measured at room temperature after cooling.	68
4-1	(a) TEM image of a functional part of the Intel fabricated PCM: SAE is the small area electrode and TI is the thermally insulating dielectric. The switching process results in a conductive crystalline filament between SAE and top electrode. (b) Typical PCM IV characteristics: 1 - conductive (crystalline) phase IV, 2 - insulating (amorphous) phase IV, 3 - switching portion, 4 - portion of IV following the threshold switching.	72

4-2	Left: evolution of the filament embryo through its primary nucleation (a), secondary nucleation events (b), and radial growth (c): arrows represent the electric field lines. Right: the free energy of the crystalline filament vs. its radius for the cases of on and off electric field. Arrows 1 and 2 represent respectively the filament radial growth and decay when the field is off (fat arrow).	73
4-3	Logarithm of switching time as a function of voltage V_D with error bars showing the standard deviation for the same device measured more than 400 times. Shown on the inset is the standard deviation of $\log \tau$	75
4-4	Block diagram of the measurement circuit for initial programming. GPIB (General Purpose Interface Bus), DAC (Digital Analog Converter), OSC (Oscilloscope) were used as the basic components in the measurement circuit.	77
4-5	Reset pulse to program the device initially	78
4-6	Sampling method for measuring R	79
4-7	Experimental set ups after the devices were initially programmed	80
4-8	Time to crystallize vs. Temperature	81
4-9	High temperature switching reflected in the resistance drop takes place after the delay times increasing with lowering the voltage V_D and the temperature T (shown to the left of the corresponding curve)	82
4-10	Voltage dependence (a) and temperature dependence (b) of switching delay time. Linear fits: Eq. (B.10).	83

4-11	(a) Stable resistance change as a function of the potential pulse width in the case of pulse triggered switching. The gradual decay of R corresponds to partial switching. (b) Normalized threshold voltage vs. the corresponding average switching time. The curve is fit by Eq. (B.9).	83
4-12	Experimental design for under threshold event	84
4-13	Long-time room temperature switching triggered by voltages well below the threshold voltage, which for the illustrated device was $V_{th} = 1.37$ V with the standard switching delay time of ~ 10 ns. Switching events took place at $V_D = 1.0$ V (left) and $V_D = 1.07$ V (right), corresponding to respectively $\tau = 29$ s and $\tau = 5$ s.	84
4-14	3D model of GST as top electrode and a metal as bottom electrode, assumed as a series network of two resistances with thermal conductivity, $K = 0$ outside the boundary and are thermally grounded at the ends	85
4-15	Temperature gradient of amorphous GST (top electrode) and a metal (bottom electrode) at different read biases ranging from 0.2v to 0.5v	85
A-1	Conceivable band diagrams of CdS based PV. (a) p-n structure with n-type CdS and p-type absorber. (b) A 'gull wing' potential shape structure; (+) and (-) mark the polarization charges. (c) The 'hunch' model where electric field in CdS region allows for carrier collection. Dot-dashed lines show the Fermi level. For simplicity, the conduction band offset between the CdS and absorber is set to zero.	88

A-2	AMPS [46] generated light $J - V$ characteristics and quantum efficiencies (QE) for three different device models: the standard p-n junction (a), gull wing potential (b), and the opposing field model(c).	90
B-1	Free energy of Eq. (B.4) as a function of the cylinder radius R and length h . The arrows illustrate possible phase transformation pathways: 1 passes through the maximum nucleation barrier, 2 follows the transformation path at fixed $\xi = h/R$ corresponding to Eq. (B.5), 3 shows that yet lower nucleation barriers may be possible.	93
B-2	Nucleation barrier of Eq. (B.5) corresponding to the transformation with fixed $\xi = h/R$ as a function of cylinder proportion ξ and field strength parameter ζ	95
B-3	Contour plot of the energy surface and nucleation pathways from Fig. B-1.	97

List of Tables

2.1 PV parameters of CdTe cells after CdCl ₂ treatment under the open-circuit (OC), forward bias (F), reverse bias (R), and short circuit (SC) conditions. Averages over 40 nominally identical cells for each condition.	43
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Chapter 1

Introduction

The modern day computerized world needs smaller size and faster speed along with less labor and sufficient energy. To meet all these requirements, a majority of tasks should be performed by small machines with large memory capacity and endurance driven by electrical power of some sort of renewable energy. The consumption of non-renewable energies has caused a huge demand to the environment. Electrical energy in the form of photovoltaics and a long cycling life, low programming energy memory device are needed in today's world.

A number of novel electricity generation methods utilizing inexhaustible (renewable) resources have been proposed and put to practise to some extent. The most promising ones are photovoltaic, wind, tidal, wave, geothermal and biomass [1]. Direct photovoltaic (PV) conversion from sunlight to electricity using large area semiconductor modules (arrays of solar cell) is one of the most promising methods. Researchers around the world have spent decades in this field in making solar energy a viable alternative.

This dissertation deals with two research areas that are typically considered mutually independent: Thin-film photovoltaics (PV) and phase change memory (PCM). In the present context, however, these two have a commonality of using the same class of materials. They are called the chalcogenide materials, and their properties are significantly different from that of the "classical" electronic materials such as Si and GaAs underlying the existing electronic devices; e.g. Si-based PV (either crystalline or amorphous), silicon transistor memory, and many others.

The latter established technologies have been recently challenged by a number of emerging electronic industries utilizing chalcogenides. In particular, the thin film PV built on two chalcogenide materials CdTe and CdS has become a product of high demand in the several past years and its production (already at the level of more than 10 billion USD) keeps growing. Another impressive application of chalcogenide is the phase change memory where high and low resistive phases of chalcogenides are used as the two logical states, and which is currently moving to its scale-up production phase supported by many key players in semiconductor devices: Intel, IBM, Numonyx, Ovonyx, Qimonda and Hynix.

With the requirement of long cycling life and low programming energy memory device in mind, PCM becomes a new contender coming to the realm of nonvolatile memory and storage.

For decades, the magnetic-disk was in the market but as the computers get smaller and require quicker storage, disk drives are lagging behind in satisfying many users needs. Flash memory has gained the most widespread in this years since in USB flash drives and memory cards within a size of a thumbnail can hold several gigabytes

of data. But as the storage and speed requirements increase, PCM is expected to replace flash memories in the market to keep up with the huge demand.

1.1 Chalcogenide Materials and their use in PV and PCM

A Chalcogenide is a chemical compound consisting of one chalcogen ion and at least one more electropositive element. The name is generally considered to mean "ore forming" from the Greek Chalkos "ore" and gen "formation".

The chalcogens are the name for the periodic table group VI (VIB or VIA) in the periodic table. It is sometimes known as the oxygen family. It consists of elements oxygen (O), Sulphur (S), Selenium (Se), Tellurium (Te), the radioactive Polonium (Po) and synthetic Ununhexium (Uuh). The compounds of the heavier chalcogens (particularly the Sulfides, Selenides and Tellurides) are collectively known as Chalcogenides. Unless grouped with a heavier chalcogen, oxides are not considered chalcogenides.

The modern technological applications of chalcogenide films are widespread from storing data electrically (Flash Memory) and optically (CD and DVD) to thin film photovoltaics (CdTe/ CdS PV and CIGS/ CdS PV). Chalcogenides form an important group of semiconductor compounds among which are well known binary compounds (CdS, CdTe) and ternary and more complex compositions such as CuInGaSe₂, Ge₂Sb₂Te₃, etc., and in addition, exhibit a number of unique features such as pyro

and piezo electricity, field induced phase transformations, and self compensation.

The phase change memory devices use chalcogenide thin films, often tellurium rich, multicomponent chalcogenide alloys of germanium, antimony, etc. The programmable random access memory (PRAM) is a non-volatile computer memory that use unique properties of chalcogenide glasses trying to take the universal market of flash memory. On the other hand, the chalcogenide based PV has successfully started gaining more and more market, inspite of the fact that many details of its operations remain poorly understood.

1.2 Piezo and Pyro coupling in chalcogenide thin film photovoltaics

The binary compounds crystallizing in the hexagonal wurtzite structures are the simplest crystals lacking a center of symmetry and, hence, capable of exhibiting piezo-electric and related effects depending on polar symmetry. The piezo electric coupling between elastic and electrical energy is of particular theoretical [5] and practical [6, 7] interest in II-VI compounds, because their conductivity can be controlled.

Two major types of polycrystalline thin-film PV based on CdTe and CuIn(Ga)Se₂ (CIGS) absorbers (Fig. 2-1) include a thin CdS layer, in which electro structural coupling exists in the form of pyro- and piezo- electricity.

Strong piezo and pyro effects present in both CdS crystals and polycrystalline thin films could be an important factor, since the CdS layer is naturally put into a device

under compression. Through the piezo effect, the compression can translate into a dipole layer type of electrical polarization and considerable static voltage across CdS films, affecting the device parameters.

CdS is a member of the crystallographic point group 6mm, it possesses three independent piezoelectric coefficients [4], including the d_{31} , which relates a stress perpendicular to the c-axis to a piezoelectric polarization parallel to that axis. This means that when the CdS grains are stressed in the lateral direction, they generate voltage across the film.

In addition, the hexagonal CdS crystalline structure exhibits a rather strong pyroelectric effect [17], with spontaneous, surface charges that are related to chemically different interfaces [18]. In the case of CdS, such are the Cd terminated (electrically more positive) and the S terminated (more negative) interfaces. The pyroelectricity can be significantly suppressed in CdS thin films due to substrate clamping (constant strain boundary condition). Such a suppression makes the pyroelectric effects seemingly piezoelectric in origin.

This dissertation particularly deals with the problem of experimental verification of the piezo- photovoltaic coupling effects in the CdS based thin film PV. This is relatively a new topic started with the recent work by D. Shvydka, et.al [9] indicating the presence of piezo- PV coupling in CdTe/ CdS structures and assuming its general significance for CdS based PV.

1.3 Phase change Memory Structural Transformations Amorphous- Crystalline

Phase change nonvolatile semiconductor memory technology is based on an electrically initiated reversible rapid amorphous to crystalline phase change process in multi component chalcogenide alloy materials similar to those used in rewritable optical disks. Chalcogenide alloys are materials containing one or more elements from Group VI of the periodic table. They are typically good glass formers in large part because Group VI elements form predominantly two fold co-ordinated covalent chemical bonds that can produce linear, tangled, polymerlike clusters in the melt. This increases the viscosity of the liquid, inhibiting the atomic motion necessary for crystallization.

All prototype devices in phase change memory make use of a chalcogenide alloy germanium (Ge), antimony (Sb) and tellurium (Te) called *GST*. It is heated to a high temperature (over 600 degree Celsius), at which point the chalcogenide melts. Once the melt is cooled, it finds itself frozen into amorphous glass like state with high electrical resistance. However , slowly heating the amorphous chalcogenide to a temperature above its crystallization point, but below melting point makes it structurally transform into a crystalline state with much lower resistance.

Two special electronic properties of a chalcogenide amorphous semiconductors alloy are required for the operation of PCM devices- the strong dependence of electrical resistivity on the structural state of the material and high field threshold switching phenomena. Polycrystalline *GST* 225 alloy has a resistivity of 3 orders of magnitude

lower than the vitreous state- sufficient to enable good memory read capability [2].

While the switching phenomenon in chalcogenide glasses has been discovered almost 50 years ago [3], its current understanding remains rather limited. Mechanism of switching from the amorphous state to the low crystalline state is yet to be established. Also, the amorphous state was found to change its characteristics over time, again without much understanding of the underlying physics. The commonality between these and the other PCM phenomena is that changing the electric field in the device results in structural transformations and vice versa, structural changes entail strong electric response. These issues will constitute another major part of the present thesis.

Chapter 2

Piezo & Pyro Photovoltaic Coupling

2.1 Introduction

Two major types of polycrystalline thin-film photovoltaics (PV) based on CdTe and CuIn(Ga)Se₂ (CIGS) absorbers (Fig. 2-1) include a thin CdS layer, [8] which empirically appears irreplaceable, even though understanding of its role remains rather poor. One hypothesis regarding the underlying physics of CdS layer is based on the recently observed pressure dependence of PV parameters in the above types of PV [9–11]. This observation was attributed to the strong piezo-effect in the hexagonal (wurtzite) phase of CdS well-known in many applications, yet overlooked in the PV community. It is known indeed that various deposition techniques create CdS films in either predominantly or considerable concentration of wurtzite phase, [12–15] which is piezo-active; the alternative cubic phase is not piezo-active and can be present as a

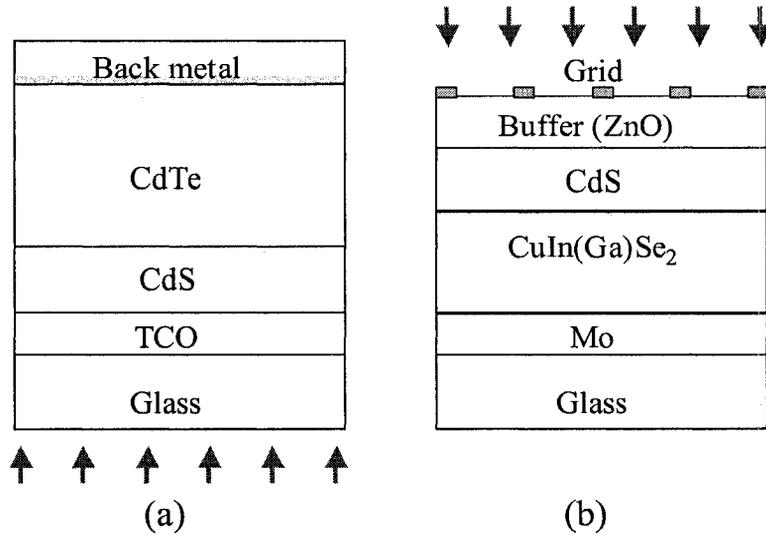


Figure 2-1: Sketch of CdTe/CdS PV cell (a) and CuIn(Ga)Se₂ PV cell (b) corresponding to the superstrate and substrate structure respectively; TCO stands for the transparent conductive oxide. Arrows show the direction of incident light.

part of mixture. The piezoelectric coupling factor [the ratio of conserved (elastic) over transformed (electrical) energy] $|k| \gtrsim 0.1$ in CdS is several times greater in absolute value than that of the crystalline quartz, a known 'classical' piezoelectric [16].

In addition, the hexagonal CdS crystalline structure exhibits a rather strong pyroelectric effect [17]. As it always takes place with the pyroelectrics, the spontaneous surface charges are related to the chemically different interfaces [18]. In the case of CdS, such are the Cd terminated (electrically more positive) and the S terminated (more negative) interfaces. The pyroelectricity can be significantly suppressed in CdS thin films due to the substrate clamping (constant strain boundary condition). Such a suppression makes the pyroelectric effects seemingly piezoelectric in origin [19].

Strong piezo- and pyro-effects present in both CdS crystals [16] and polycrystalline

thin films [19, 20] could be an important factor, since the CdS layer is naturally put in device under compression. Through the piezo-effect, the compression can translate into the dipole layer type of electrical polarization and considerable static voltage across the CdS film affecting the device operations.

Another reason to expect a strong effect of piezo-electric polarization in CdS is its similarity with the known phenomenon of anomalous PV effects in ferroelectrics, [21, 22] where the internal electric field effectively separates the photogenerated electron-hole pairs leading to an extremely strong photovoltage.

From the practical standpoint, the latter consideration opens a possibility of device tuning by properly adjusting the compression. Various adjustments can be conceivably achieved in several ways, for example, (1) by changing the tangent layer morphology, in particular the morphology of transparent conducting oxide (TCO) or various buffer layers [8] tangent to CdS; (2) changing the CdS deposition parameters thereby affecting its grain geometry and related mechanical stress; (3) via postdeposition treatments that can relax or increase the stress in CdS thereby changing its electrical polarization; (4) by direct electric field application aimed at aligning the electric dipoles corresponding to the individual grains of CdS layer. These and possibly some other venues of PV engineering related to the piezo- and pyro- effects in CdS so far have not been systematically explored.

On the other hand, from the academic perspective, the piezo- or pyro- active CdS coupled to the photo-voltaic structure forms a new type of system that appears quite nontrivial. Indeed, since the strained CdS grains behave as electric dipoles, they will tend to align in the PV electric field. In its turn, the latter will depend on the electric

properties of the CdS layer. This results in a system of strongly coupled photo-voltaic and piezo-electric, which to the best of our knowledge has never been considered.

One particular consequence of the above mentioned CdS polarization is that the 'mainstream' understanding of CdS based PV as p-n junction ceases to apply. Instead, the electric potential distribution across the semiconductor junction can become non-monotonic with field reversal in the CdS region as shown below.

It is believed that the above sketched practical and scientific problems, form a field of its own calling upon many independent contributions to become fully developed. This work is aimed at summarizing the results and understanding, as well as pointing at many remaining challenges and uncertainties.

The semiconductor thin-film structures containing pyro- and piezo-electric junctions are known in other applications, such as ferroelectric memories, [23,24] electronic and photonic devices based on nitride materials systems [25], and CdS polycrystalline films on flexible substrates and threads [26,27]. These applications triggered new insights into thin film device physics including screening of pyroelectric films and grains in semiconductor matrix [28,29]. In other words, the concepts of pyro- and piezo-active thin-film structures are not entirely new from a broader perspective, it is just due to a certain combination of factors that they have not been given enough consideration in the physics of thin-film photovoltaics.

2.2 Physical aspects of piezo-photovoltaics

A theoretical discussion in this dissertation is limited to several basic questions pertaining to the physics of piezo- and pyro-electric effects in polycrystalline PV structures with the understanding that this dissertation is primarily of experimental field. It will become apparent from what follows that these effects have a degree of complexity beyond the existing understanding of photovoltaic and piezo-electric phenomena. Therefore the discussion here is limited mostly to a qualitative description of what happens when one layer in a photoactive structure generates the electric polarization due to pyro- or piezo- effect in its grains.

2.2.1 Characteristic parameters

The grains in a polycrystalline CdS film are put under lateral compression already due to the nature of the film deposition where nucleation and growth of individual grains make them compete for material and volume. Other factors potentially contributing to the internal stress include lattice mismatch between differently oriented grains of CdS, as well as between the grains of CdS and those of the tangent layers, such as CdTe, CIGS, TCO, or ZnO in Fig. 2-1.

The CdS film thickness and grain sizes vary between different technologies in the range of 0.05 to 0.2 μm and 0.01 - 0.2 μm respectively [8,12,14,31]. In the hexagonal phase, a preferential orientation (002) (along Z axis, called also *c*-axis in Fig. 2-2) is typically observed (see also Sec. 2.3.3 below). However, there is evidence [27,36] of smaller, \sim 3-5 nm in diameter, single crystal sub-grains of different orientations

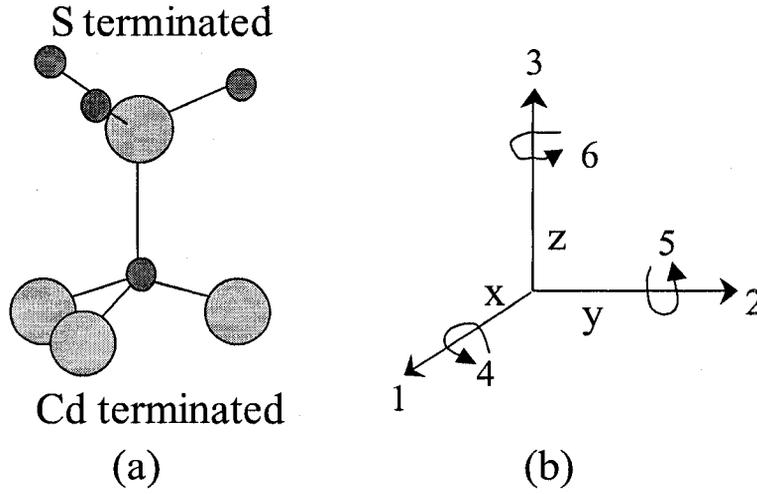


Figure 2-2: (a) Piezoelectric element of the hexagonal CdS structure showing predominantly Cd and predominantly S terminated planes. (b) Direction of forces affecting the piezoelectric element. Directions X, Y, or Z are represented by the subscript 1, 2, or 3, respectively. Shears about these axes are represented by the subscripts 4, 5, or 6 respectively.

forming the individual grains in polycrystalline CdS films.

The lateral strain (i.e. the relative volume change) can be estimated from the available XRD data as $\epsilon \sim 0.002$ [32, 33]. Through the piezo-effect, (illustrated in Fig. 2-3) it translates into electric polarization

$$P_i = d_{ij}T_j \quad (2.1)$$

(in the IEEE standard notations [34]). Here d_{ij} is the piezo-electric tensor relating the polarization P_i to the stress T_j . For the hexagonal structure of CdS, the following

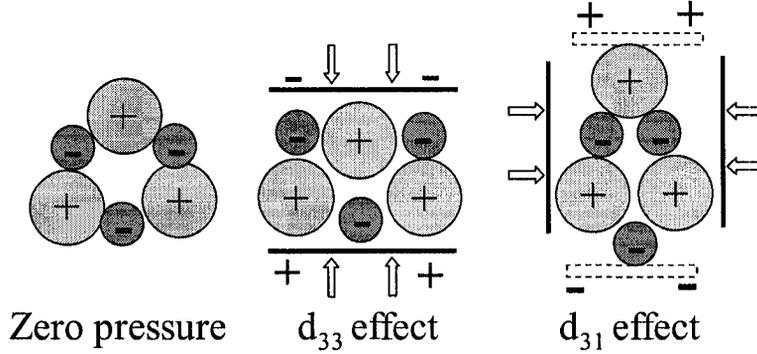


Figure 2-3: Sketch of the mechanisms of piezo-electric polarization along Z axis in response to the stress (shown by arrows) parallel to Z axis (d_{33} effect) and to X axis (d_{31} effect).

elements of that tensor have non-zero values [16] (in 10^{-12}C/N):

$$d_{33} = 10.32, \quad d_{31} = d_{32} = -5.18, \quad d_{15} = d_{24} = -13.98.$$

where the first and second indices give respectively the direction of polarization and the direction of stress (including shear stress) as illustrated in Figs. 2-2 and 2-3. This can be summarized as $|d_{ij}| \sim 10^{-11} \text{ C/N}$, which is by at least one order of magnitude larger in absolute value than that of CdTe and many other semiconductors [16].

For numerical estimates it is assumed [16] the in-plane stress (perpendicular to the c axis) $T_1 = c_{11}\epsilon \sim 2 \cdot 10^8 \text{ N/m}^2$ for the above ϵ and the elastic constant $c_{11} \approx 10^{11} \text{ N/m}^2$. The polarization and voltage along Z axis in Fig. 2-2, i. e. across the film, is then determined by $d_{31} \approx 5 \cdot 10^{-12} \text{ C/m}^2$. In particular, the surface charge density corresponding to these parameters and polarization in Eq. (2.1) is of the order of $\sigma = P_n \approx 10^{12} \text{ e/cm}^2$ where P_n is the normal component of polarization and e is the

electron charge. This charge density will generate a strong electric field

$$\mathcal{E} = 4\pi\sigma/\varepsilon \sim 10^5 \text{V/cm} \quad (2.2)$$

where $\varepsilon \approx 10$ is the dielectric permittivity of CdS.

Assuming uniform polarization, the voltage across the CdS layer can be expressed as

$$V_i = d_{ij}T_j/C_0, \quad (2.3)$$

where C_0 is the layer capacitance per unit area. The geometrical capacitance $C_0 \approx 4 \cdot 10^{-4} \text{ F/m}^2$ corresponding to the film thickness of $0.2 \mu\text{m}$. This yields $V_1 \sim 5V$. The latter voltage is 'abnormally' high exceeding the CdS forbidden gap $G \approx 2.4 \text{ V}$, which is physically impossible as leading to the electric breakdown and a high concentration charge carriers screening the voltage.

To estimate the *spontaneous* (pyroelectric) polarization in CdS, the known surface charge density [16] for this material $\sigma \approx 0.09 \mu\text{C/cm}^2$ at room temperature corresponding to the electron charges density $\sim 10^{12} \text{ e/cm}^2$, the same number as the above estimated piezo-induced σ . From this it can be concluded that the pyroelectric polarization is significant potentially leading to the voltage drop comparable to G across the typical CdS thickness films.

2.2.2 Internal screening

Piezo- and pyro-electric fields can be significantly screened in the CdS grain by properly redistributing mobile electric charges, either existing due to doping or field generated as illustrated in Fig. 2-4. Both highly conductive CdS layers [13] with charge carrier concentration $N \sim 10^{19} \text{ cm}^{-3}$ and highly resistive CdS layers close to intrinsic [8,35] have been reported in the literature, leading to the respective screening mechanisms in Fig. 2-4 (a) and (b).

For the case (a) the electric polarization produces the voltage drop estimated as

$$\delta V = \mathcal{E}L_0/2 \ll G/e \quad (2.4)$$

where L_0 is the screening length and the coefficient of 1/2 accounts for the difference between the boundary and the average values of the electric field. Given doping concentration N the screening length becomes

$$L_0 = \frac{\sigma}{Ne}. \quad (2.5)$$

Substituting here the above estimated $\sigma \sim 10^{12} \text{ e/cm}^2$ and the highest known $N \sim 10^{19} \text{ cm}^{-3}$ gives $L_0 \sim 0.1 \text{ } \mu\text{m}$ and $\delta V \approx 0.5 \text{ V}$. For the typical resistive CdS layers one can use $N \sim 10^{13} - 10^{14} \text{ cm}^{-3}$ leading to $L_0 \sim 0.1 - 1 \text{ mm}$.

For the case (b) it is understood that the band bending δV in Eq. (2.4) exceeds half of the band gap, which triggers strong charge accumulation screening the electric field. The condition for this regime is $e\delta V \gtrsim G/2$. The maximum integral electric

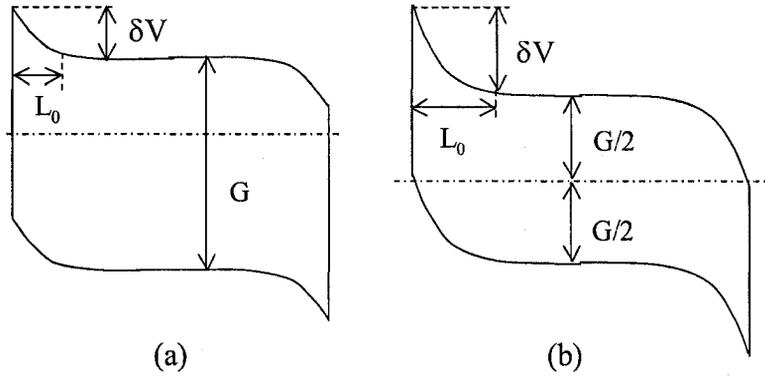


Figure 2-4: Screening of the piezo- and pyro-electric fields in CdS in the cases of strongly doped (a) and intrinsic (b) uniform materials.

potential drop across the system is close to G/e corresponding to the maximum polarization of

$$P_{max} = \sqrt{\frac{\epsilon GN}{4\pi e^2}}. \quad (2.6)$$

As a numerical example, P_{max} corresponds to the surface charge density $\sigma/e \sim 3 \cdot 10^{11} \text{ cm}^{-2}$ for the case of highly resistive CdS with $N \sim 10^{14} \text{ cm}^{-3}$.

It follows from the above estimates that even in the case of strongly doped CdS, the screening length either exceeds or is comparable to the grain linear size, which is typically below 200 nm. Therefore, the internal screening can decrease the estimated 'abnormal' electric potential drop by a numerical factor, but not the order of magnitude, say from 5V to 2 V for a 200 nm uniformly polarized grain.

The electric charges of surface states present another factor that can reduce the piezo- or pyroelectric voltage drop across the CdS grain. A noticeable reduction takes place when the surface state density is comparable to the above estimated $\sigma/e \sim 10^{12} \text{ cm}^{-2}$; such surface charge densities are realistic [37] However, the effect of

surface states will depend also on their energy spectrum and remains hard to estimate numerically. In general, the case of surface states compensating the polarization charges exactly, would appear a sheer coincidence. It seems more natural to expect some fractional compensation retaining the order of magnitude of the polarization induced voltage.

The above mentioned random composite structure [Fig. 2-5 (a)] combining $M \gg 1$ differently oriented nanocrystals can have a strong effect on the grain polarization. Assuming for simplicity a completely random nanostructure orientation, the average grain polarization becomes zero, while its characteristic fluctuation can be estimated as

$$\delta P = \frac{p\sqrt{M}}{R^3} = \frac{P}{\sqrt{M}} = P\sqrt{\frac{r}{R}} \ll P \equiv \frac{pM}{R^3} \quad (2.7)$$

where p is the average absolute value of the dipole moment of one nanocrystal, P is an unscreened polarization corresponding to the case when all the dipoles are aligned, and r and R are the linear sizes of a nanocrystal and a grain respectively (note that in reality the polarization P may not be allowed due to the charge carrier screening). As a result the polycrystalline film becomes an ensemble of randomly polarized grains of the characteristic absolute value of polarization δP estimated in Eq. (2.7).

Using $r \sim 5$ nm and $R \sim 200$ nm gives $\delta P \sim 0.15P$ thus reducing the voltage drop across the grain from 5 V to less than 1 V. Some less likely configurations of nanocrystals can still have higher integral dipole moments up to the maximum polarization P_{max} consistent with the charge carrier screening.

In summary, the 'internal' screening mechanisms result in an ensemble of grains

that can have various polarizations ranging from zero to P_{max} depending on CdS parameters, such as doping, grain size, etc. They can be either randomly oriented or somewhat aligned due to preferential growth directions. We shall see in what follows that in the case of originally random orientation the system of grain dipoles still can be polarized due to its interaction with the tangent semiconductor layer [CdTe or CuIn(Ga)Se₂].

Note that even assuming the internal screening to cause an order of magnitude reduction of our originally estimated polarization voltage $\sim 5V$ across the CdS film, its remnant value $\sim 0.5 V$ remains comparable to the device open-circuit voltage $V_{oc} \sim 0.5-0.8 V$ and cannot be neglected. It might be due to some masking factors (such as, CdS surface coupling with the tangent layers and ambient, surface contaminations, and shunting) that the piezo-coupling was not detected in much of the previous work [30].

2.2.3 External screening

Given enough time and high temperature, the dipoles of polycrystalline film grains can align in the external electric field [Fig. 2-5 (b)] to decrease the electrostatic energy of the system. Such a field in photovoltaic structures is purposely created in order to separate the photogenerated electrons and holes. Two opposite scenarios are considered corresponding to (1) fixed, generally nonequilibrium dipole polarization independent of the surrounding material feedback, and (2) the equilibrium dipole polarization established at a given temperature so as to minimize the system free

energy. The former case corresponds to the assumption that the dipole layer was formed in the course of structure deposition or high temperature treatment and cannot depolarize thereafter. The latter limiting case implies high enough temperatures or other special conditions that make it possible for the grain dipoles to rearrange.

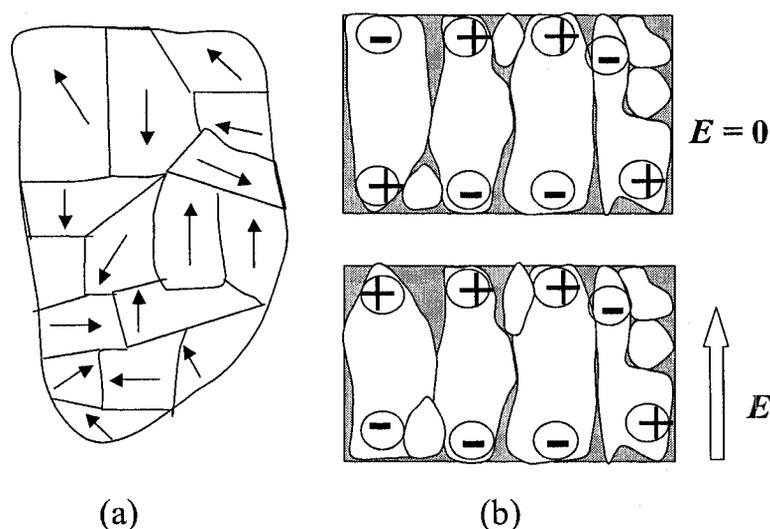


Figure 2-5: (a) Sketch of CdS grain composed of many randomly oriented nanocrystals; arrows showing their electric polarizations. (b) Top: randomly polarized grains forming a film with zero average polarization. Bottom: Grain alignment in the external electric field leading to a film with finite polarization

Screening of a fixed polarization

Following the recent analysis in Ref. [28, 29], consider a thin film with a fixed transversal polarization (such as a pyroelectric film) in contact with a non-polar semiconductor. The mobile charges will move to screen the film polarization thereby making the semiconductor polarized in the opposite direction (Fig. 2-6).

The two limiting cases shown in Fig. 2-6 lead to significantly different screening

lengths. In the case (a) the pyroelectric film thickness l is much larger than the depletion width L . The system behavior can be understood as a result of trying to minimize the total electrostatic energy, hence, suppressing the electric field in its largest component, which is the pyroelectric film for the case (a). This is achieved by stronger coupling the positive (negative) polarization charge in the film with the negative (positive) polarization charge in the tangent material. In particular, the semiconductor experiences only the electric field of the closest polarization charge in the film. Its neutralization results in the screening length L defined in Eq. (2.5), but with N corresponding to the non-polar semiconductor.

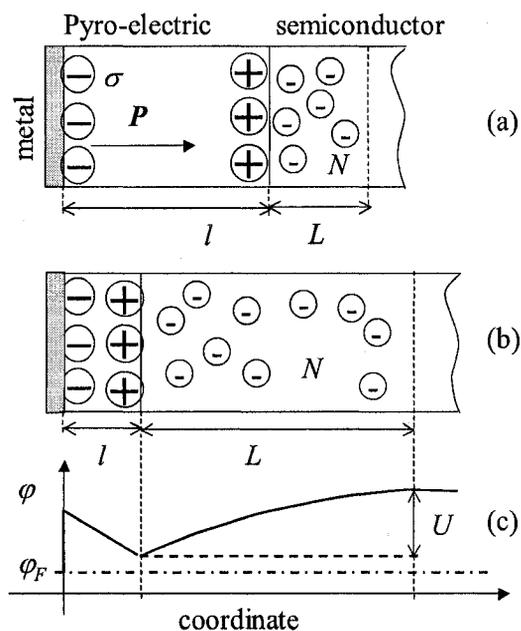


Figure 2-6: (a) Sketch of electric charge distributions in a structure of metal-pyroelectric film-semiconductor for the case when the screening (depletion) length in semiconductor is much greater than the film thickness l . The metal polarization charge is not shown. \mathbf{P} is the vector of polarization. (b) The same for the opposite limiting case $l \ll L$. (c) The equilibrium electron potential energy for the case (b). ϕ_F is the Fermi potential.

In the opposite limiting case (b) $l \ll L$ (referred to as the dipole screening [28,29]) the field in the pyroelectric film is almost unaffected by the semiconductor polarization, the latter being much weaker than that of the case (a) thereby suppressing the electrostatic energy in the largest part of length L . In that case, the semiconductor polarization is governed by the film dipole Pl rather than the charge σ . The balancing dipole moment of the semiconductor depleted layer can be written as the product of the depleted region charge NeL times the average distance $L/2$. Equating the two dipole moments yields the screening length

$$L = \sqrt{\frac{2Pl}{eN}}.$$

A more exact consideration [29] takes into account the difference between the dielectric permittivities of pyroelectric film ϵ_p and tangent semiconductor ϵ_s , yielding

$$L = \sqrt{\frac{2Pl \epsilon_s}{eN \epsilon_p} - \frac{\epsilon_s V}{2\pi eN}} \quad (2.8)$$

where V is the electric potential difference between the semiconductor rightmost point and the metal. [38] The band bending U in Fig. 2-6 is given by

$$U = \frac{4\pi Pl}{\epsilon_p} - V. \quad (2.9)$$

The electron potential difference across the pyroelectric film is expressed as

$$V_P = \mathcal{E}_p l = \frac{4\pi Pl}{\epsilon_p} \left(1 - \frac{l \epsilon_s}{L \epsilon_p}\right) + \frac{\epsilon_s V l}{\epsilon_p L}. \quad (2.10)$$

It is straightforward to see that corresponding to the parameters of practical interest in thin-film PV is the inequality $l \ll L$ (typically $l \sim 0.1 \mu\text{m}$ and $L \gtrsim 1 \mu\text{m}$), hence, the latter dipole screening regime applies determining the built-in field and charge carrier collection in the space-charge region of the semiconductor.

Note that the above consideration and Eq. (2.8) are limited to the case of not too strong band bending where the screening is due to the depletion and not the minority carrier accumulation. The latter condition can be close to violation given a set of conceivable CdS parameters, such as $\epsilon_p \approx 10$, $l \approx 0.1 \mu\text{m}$, and the maximum polarization $P \approx \sigma \sim 10^{12} \text{ e/cm}^2$, for which Eq. (2.8) predicts $L = 0$ when $V \sim 1 \text{ eV}$. Because the latter voltage is comparable to the semiconductor band gap ($G/e \approx 1.5 \text{ V}$ in CdTe and $G/e \approx 1.2 \text{ V}$ in CuIn(Ga)Se₂) we conclude that the band bending in a semiconductor can be strong.

Another interpretation of the condition $L = 0$ is that it determines the point of shorting the space charge region and therefore can be thought of as the open circuit voltage, $V = V_{oc}$ condition. The observed V_{oc} are indeed of the predicted range ($\approx 0.8 \text{ V}$ in CdTe and $\approx 0.6 \text{ V}$ in CuIn(Ga)Se₂) pointing at their possible relation to the CdS polarization.

The opposite limiting case of the accumulation regime screening can be described as well [29, 39] leading to much shorter screening lengths and weaker electric fields.

The screening length in Eq. (2.8) suggests a new interpretation of the standard capacitance-voltage ($C - V$) data, since $C \propto 1/L$ and L contains the film polarization never taken into account in the preceding work .

Equilibrium polarization

The existing PV technologies include high-temperature processing steps such as, for example, the high temperature CdCl_2 treatment of CdTe based PV [8]. The electric dipole equilibration at high enough temperatures may result in considerable orientational disorder [40] affecting the CdS dipole layer. Here we consider the equilibrium dipole polarization due to interaction with the tangent semiconductor layer (CdTe or $\text{CuIn}(\text{Ga})\text{Se}_2$) and metal electrode assuming that the dipoles are free to align in the external field.

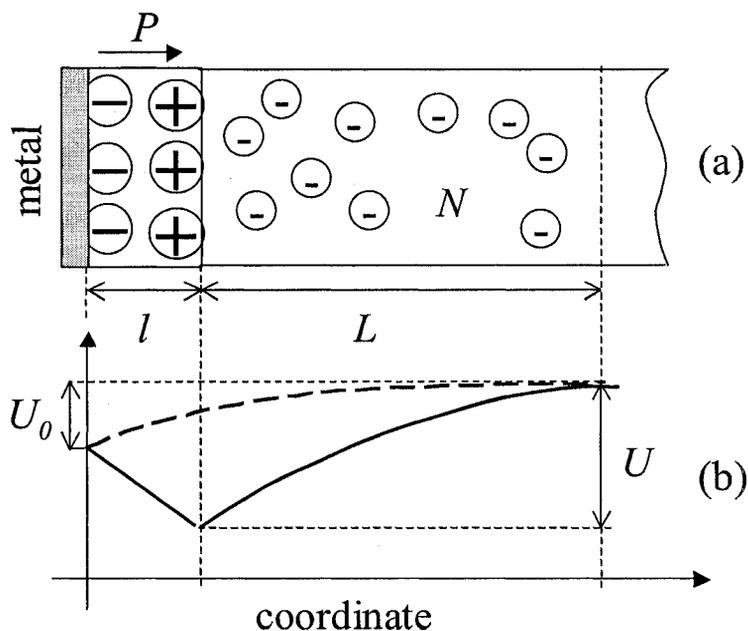


Figure 2-7: (a) The electric charge distribution in a structure of metal - pyroelectric film - semiconductor; the metal polarization is not shown. (b) The electron potential energy for the case when there is no pyroelectric film (dashed line) and for the case when the film is present. Not to scale: $l/L \ll 1$.

The qualitative understanding is illustrated in Fig. 2-7. Corresponding to the

'standard' PV effect is a non-polarized ($P = 0$) film and certain 'bare' built-in potential U_0 . The latter can drive the electric current of photogenerated electrons and holes. The 'open-circuit' voltage $V_{oc,0} \approx U_0$ needed to block that current is a major PV parameter sought to be made as high as possible. When allowed to align, the film dipoles create polarization P , the corresponding partial field reversal, and the gull-wing shaped potential with the barrier $U > U_0$. The amplification $U/U_0 > 1$ translates into a higher open circuit voltage $V_{oc} \approx (U/U_0)V_{oc,0}$. More quantitatively, the effect of gull-wing potential on the open circuit voltage and other PV parameters is analyzed in Appendix A.1 below.

The analysis of the free energy is similar to that of Ref. [41] dealing with a thin ferroelectric film sandwiched between a metal and a semiconductor. The system's free energy is written in the form [42]

$$F = F_0 - (1 - \alpha) \int_0^P \mathcal{E}_p d(Pl) + \frac{\epsilon_s}{8\pi} \int_0^L \mathcal{E}_s^2 dx. \quad (2.11)$$

Here the first term accounts for the deformation energy, the second term describes the film dipole (Pl) in the field \mathcal{E}_p , and the last term represents the energy of the space charge region of width L .

An important difference between the present analysis and that of Ref. [41] is the coefficient $0 < \alpha < 1$ (absent in Ref. [41]), which describes the relative decrease in polarization energy due to the metal electrode, similar to the well-known metal effect on a point charge energy. This effect readily described in the terms of image charges may seem counterintuitive as applied to the case under consideration because a dipole

layer does not generate the outside electric field. We note however that the latter property is characteristic of infinitely large area layers only. For the case of a finite area layer, the electric field inevitably appears at its edges inducing the formation of an image dipole layer as illustrated in Fig. 2-8. Since the polarization builds up by finite size portions, over time the integral dipole layer will have multiple edges sufficient to create the metal polarization representable by image dipoles. We note that while the image dipole layer does not generate any electric field, it contributes to the electric potential.

The latter effect exists beyond the point dipole approximation. Indeed, by integrating the dipole-dipole interaction energy

$$\frac{1}{r^3} \left[\mathbf{p}_1 \cdot \mathbf{p}_2 - \frac{3(\mathbf{p}_1 \cdot \mathbf{r})(\mathbf{p}_2 \cdot \mathbf{r})}{r^2} \right]$$

with $\mathbf{p}_1 = \mathbf{p}_2$, it is straightforward to verify that the energy of interaction of two continuous parallel point dipole layers is zero. However, introducing discreteness via finite distances between the same layer dipoles (and replacing the integration with summation) leads to the negative finite interaction energy between the layers. It is clear from the physical picture of grain dipoles that the continuous point dipole approximation does not apply, since the inter-grain distances are comparable to their sizes. Therefore one can expect the negative interaction energy between the grain dipoles and the metal plate.

In general, the energy of interaction between the real and image dipole layers is quadratic in polarization. Therefore it is proportional to the bare energy of the dipole

layer, but has the opposite sign as reflected in the above choice of α . The numerical value of α of the order of several tenths turns out to be sensitive to the details of the dipole structure beyond the point dipole approximation, which will be discussed elsewhere.

Following Ref. [42], the field in the space charge region is given by $\mathcal{E}_s = 4\pi eN(x - L)/\epsilon_s$ where Ne is the charge density and x is the linear coordinate. The field \mathcal{E}_p in the dipole layer is described by either side of the equation

$$\frac{4\pi}{\epsilon_p}(eNL - P) = \frac{1}{l} \left(U_0 - \frac{2\pi eNL^2}{\epsilon_s} \right) \quad (2.12)$$

where the left- and right-hand sides represent respectively the boundary condition for the electric displacement and the distribution of the electric potential.

It is assumed that F_0 is mostly due to intergrain interactions that do not depend on P , such as the intergrain deformation, grain boundary states, etc. Therefore we neglect $\partial F_0/\partial P$ in the equilibrium condition $\partial F/\partial P = 0$, which then yields

$$\frac{2\pi eNL^2}{\epsilon_s}(1 - \alpha + \delta) - U_0 = 0, \quad \delta \equiv \left(1 + \frac{\epsilon_p L}{\epsilon_s l} \right)^{-1}. \quad (2.13)$$

Eqs. (2.12) and (2.13) fully describe the system.

The practically relevant inequality $\delta \ll \alpha$ simplifies the results

$$L = \sqrt{\frac{2Pl \epsilon_s}{Ne \epsilon_p \alpha}}, \quad P = \frac{\alpha \epsilon_p U_0}{1 - \alpha 4\pi l}, \quad U = \frac{U_0}{1 - \alpha}. \quad (2.14)$$

We observe indeed the amplification $U > U_0$ (Fig. 2-7). In addition, we point again

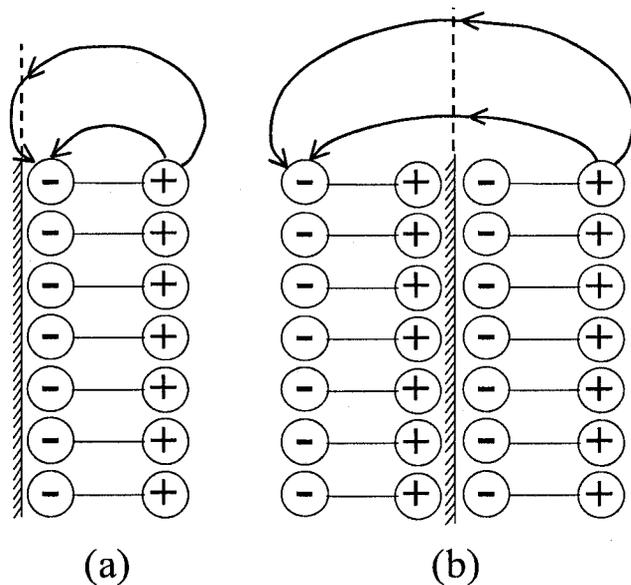


Figure 2-8: (a) The dipole layer and its electric field lines having components parallel to the metal surface. (b) The dipole layer and its image charge generate the electric field, which lines are perpendicular to the surface.

at a non-monotonic 'gull-wing' shaped electric potential distribution that appears as a result of electric dipole polarization in the CdS film.

Once the 'high-temperature' equilibrium grain polarization is established and the temperature decreased, it remains frozen, with the electric potential distribution described by the equations of the preceding section. We note also, that the heights of the left - and the right - wing barriers in Fig. 2-6 under zero bias V are the same to the accuracy of corrections linear in $l/L \ll 1$; the barrier heights under finite biases V are described by Eqs. (2.9) and (2.10). One consequence of the latter is that the CdS related barrier in the band diagram is of the order of the measured V_{oc} that is $\lesssim 1$ V.

As a brief general summary, the above consideration shows that a film made of

pyroelectric grains (such as CdS) can exhibit a ferroelectric behavior with strong polarization in response to a small electric perturbation.

The assumption that polarization by grain rearrangement requires high temperatures and flux agents promoting recrystallization can explain the role of high temperature CdCl₂ treatment of CdTe based PV improving V_{oc} , [8,43] whose mechanism remained poorly understood: It is believed that the CdCl₂ treatment helps to achieve the equilibrium polarization of CdS grains, which improves V_{oc} . To verify this understanding an experiment with CdCl₂ treatment under external bias was carried out by Dr. Diana Shvydka (see Sec. 2.3.3) and found that the bias has a noticeable impact on that treatment results. In CuIn(Ga)Se₂ technology the postdeposition anneal is known to improve the device as well. Eliminating the CdS layer from the structures [44] typically lowers V_{oc} by 30-50 %, consistent with the prediction in Eq. (2.14) when $\alpha \sim 0.3 - 0.5$.

The above consideration suggests that annealing the CdTe cell under reverse bias can increase the CdS electric field and its related barrier. This in turn will strongly increase the integral series resistance thereby ruining the device fill factor (see Sec. A.1 below) and performance. This prediction is consistent with the experimental data [45].

In conclusion, both the cases of fixed and equilibrium polarization are consistent with the available data, and neither can be ruled out at this point, both predicting the CdS barrier $\lesssim 1$ V. It is possible that in reality the intermediate case of partial equilibration is more relevant implying that some fraction of grains have the rearrangement (recrystallization) barriers low enough to occur over the time of high

temperature treatment, while other dipoles remain fixed. This uncertainty calls upon more experimental work with purposely applied electric fields, varying and cycling temperatures and stresses, and different grain morphologies.

2.3 Experimental

Several types of experiments were conducted aimed at inducing changes in PV parameters of CdS based solar cells in response to mechanical stress application. Shown in Figs. 2-9, 2-10, and 2-11 are three experimental setups aimed at exerting mechanical stresses corresponding to the device squeezing, bending, and flexing. The substrate, superstrate and flexible substrate structures were used. The setups and their corresponding data are discussed.

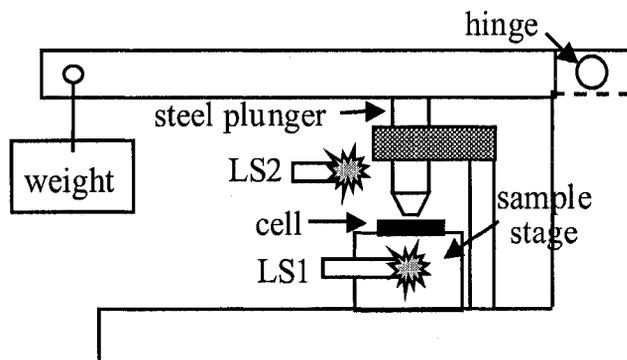


Figure 2-9: Sketch of apparatus used in our squeezing experiments for applying pressure perpendicular to the face of thin-film PV cell. LS1 (under the cell stage through the fiber optics) and LS2 show the two positions of light source used respectively in the cases of superstrate and substrate cell configurations.

2.3.1 Piezo-effect setups

Squeezing experiments

For the case of squeezing, [9–11, 30] the pressure applied normally on the device face changes linearly with the weight attached to the lever and was estimated from the

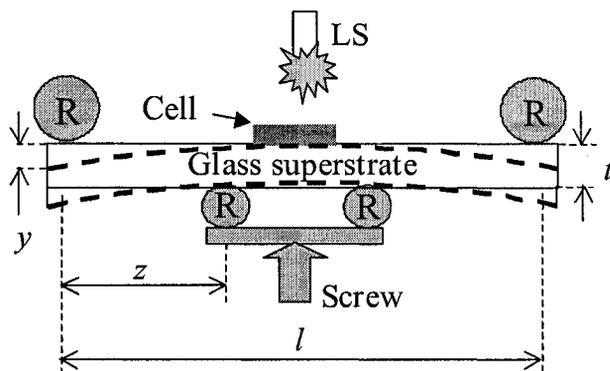


Figure 2-10: Sketch of apparatus used in our bending experiments with glass superstrates for applying stress parallel to the face of thin-film PV cell. R-labelled circles stand for the cylindrical metal rods perpendicular to the plane of the diagram. LS denotes the light source.

standard torque balance. Two different positions of light source in Fig. 2-9 were used for the superstrate (LS1) and substrate (LS2) devices sitting on the sample stage front surface down and up respectively and allowing for the pressure application directly on the semiconductor film.

It is typical of squeezing setup designs to have force exerted locally against a relatively small area of a much larger photovoltaic cell with equipotential electrodes. In such a case, the unstressed area will generate its own photo-voltage, which will partially balance the piezo-electric voltage making the device operate as two cells connected in parallel, one with lower (affected) $V_{oc1} = V_{oc} - \delta V$ and another with higher voltage $V_{oc2} = V_{oc}$. The integral measured voltage can be expressed as

$$\begin{aligned}
 V &= -\frac{AkT}{q} \ln \left[s_1 \exp \left(-\frac{qV_{oc1}}{AkT} \right) + s_2 \exp \left(-\frac{qV_{oc2}}{AkT} \right) \right] \\
 &= V_{oc} - \frac{AkT}{q} \ln \left[1 + \frac{s_1}{s_1 + s_2} \exp \left(\frac{q\delta V}{AkT} \right) \right]
 \end{aligned} \tag{2.15}$$

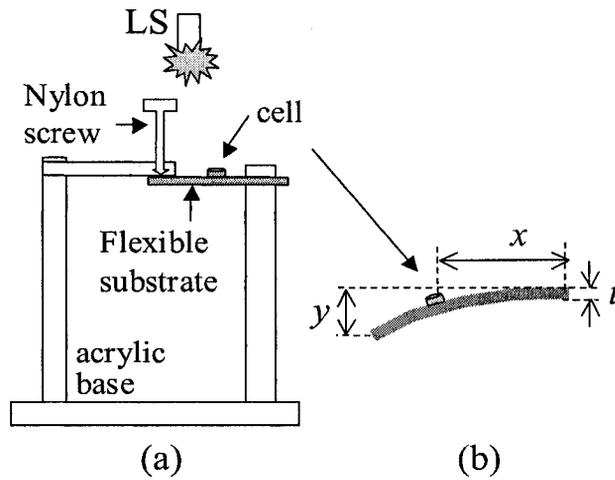


Figure 2-11: (a) Sketch of apparatus used in our flexing experiments for applying stress parallel to the face of thin-film PV cells made on flexible substrate. LS denotes the light source. (b) Geometrical dimensions of flexing experiment; y is the arrow of bending.

where s_1 and s_2 are the relative areas of the two components, and A is the ideality factor.

For normal pressure \mathcal{P} in squeezing experiments one can use Eqs. (2.3) and (2.5) to write

$$\delta V = \frac{d_{33}\mathcal{P}}{C_0} \frac{L_0}{L_0 + l}, \quad (2.16)$$

for the voltage change across the CdS layer where L_0 and l are respectively its screening length and the thickness; the multiplier $L_0/(L_0 + l)$ approximates between the cases of strong ($L_0 \ll l$) and weak ($L_0 \gg l$) screening. This yields, for the two limiting

cases, the measured V_{oc}

$$V = V_{oc} - \frac{AkTs_1}{q(s_1 + s_2)} \exp\left(\frac{q\delta V}{kT}\right), \quad \mathcal{P} \ll \mathcal{P}_c; \quad (2.17)$$

$$V = V_{oc} - \delta V + \frac{AkT}{q} \ln\left(\frac{s_1}{s_1 + s_2}\right), \quad \mathcal{P} \gg \mathcal{P}_c. \quad (2.18)$$

where

$$\mathcal{P}_c \equiv \frac{C_0 kT}{d_{33}q} \ln\left[\frac{q\delta V(s_1 + s_2)}{AkTs_1}\right]. \quad (2.19)$$

Therefore we expect the voltage to change rather insignificantly in the small pressure region $\mathcal{P} \ll \mathcal{P}_c$, while it becomes linear in \mathcal{P} for higher pressures $\mathcal{P} \gg \mathcal{P}_c$. Corresponding to our setup parameters was the characteristic pressure $\mathcal{P}_c \sim 10^7$ N/m².

Since CdS can be photoconductive, [53] its charge density and screening length L_0 will depend on the light intensity. Correspondingly, the characteristic pressure \mathcal{P}_c is expected to logarithmically increase with the light intensity as seen from Eq.(2.19).

The squeezing setup is more suitable for the superstrate configuration (CdTe PV, sunny side of cell down, light source LS1). The substrate configuration setup in Fig. 2-9 had a significant problem of light shading by the pressure applicator. Under such shading, the device still operates as two cells connected in parallel. However, the open-circuit voltage difference is given by

$$\delta V = \delta V_0 + \frac{d_{33}\mathcal{P}}{C_0} \frac{L_0}{L_0 + l}, \quad (2.20)$$

where δV_0 is due to the shadowing. Since $s_1 \lesssim s_2$, one would expect a relatively small change in the integral V_{oc} . A related conclusion is that the change should be stronger

at lower light intensities, when the background V_{oc2} value is lower.

In all cases, glass breakage set significant limits to the repeatability of our experiments (we have mostly used fresh samples to avoid this problem). In addition, for the case of superstrate configuration the pressure applicator could occasionally damage the metal contact leading to permanent device failure.

Bending experiments

Bending creates the in-plane stress, i. e. in the direction of a "natural" thin-film CdS layer stress, built-up as a result of solar cell fabrication.

Our testing set up for solar cells on glass is designed after the 4-point modulus of rupture (MOR) test, Fig. 2-10. Two smooth rods push up from below as two other smooth rods push down from above, holding the solar cell. The screw is tightened slowly pushing the bottom rods up and bending the cell. Light is directed through the glass substrate and J-V measurements are made at different glass edge deflection positions. The solar cell can face down, resulting in lateral compression of the cell, or up (as shown in Fig. 2-10), resulting in the lateral tension, effectively similar to the pressure perpendicular to the cell as an outcome of the bending of the superstrate.

The main advantage of this new bending setup is that, unlike our previous experiment, the cell under investigation is not in direct contact with pressure applicator. Therefore, this method is supposed to be less destructive to the contact. In particular, the possibility of shunting through the applicator, of a major concern with the squeezing set-up, is no longer an issue.

The lateral stress $\mathcal{P}_{//}$ was estimated based on the glass deflection measured with

a high-precision digital micrometer. More specifically, standard elasticity theory [54] gives

$$\mathcal{P}_{//} = E_{\text{CdS}} \frac{\delta l}{l} = E_{\text{CdS}} \beta \frac{t}{2} = E_{\text{CdS}} \frac{ty}{l^2} \quad (2.21)$$

where $E_{\text{CdS}} \approx 23$ GPa is the CdS Young's modulus, β is the deflection angle, $\delta l/l$ is the film relative deformation, and other notations are explained in Fig. 2-10.

Similar to the previous experiments, the amount of stress on CdS is limited by glass breakage. One noticeable difference is that here the range of stresses developed in CdS film, was on average three orders of magnitude lower than that in the squeezing experiments. This difference reflects the fact that the glass superstrate turned out to be much more brittle when subjected to bending.

It is estimated that the compressive stress \mathcal{P}_G in the glass substrate following the known MOR formula

$$\mathcal{P}_G = \left| \frac{3E_G ty}{a(3l - 4a)} \right|$$

where $E_G \approx 70$ GPa is elastic modulus of the glass and the dimensions are illustrated in Fig. 2-10. So estimated stress in the glass was of the order of 10^5 N/m². By way of comparison, the amount of stress necessary to break 50 % of glass defined by its modulus of rupture, is of the order of 10^7 N/m² for a 3 mm soda-lime glass used in our devices, which is much higher than our attained values. It is speculated that the abnormal fragility of glass in our experiments is caused by the underlying process of solar cell fabrication including heating and cooling. For example, when a piece of the superstrate with only TCO on it (i. e. as received from the vendor, prior to cell fabrication) was put in our bending apparatus, the stress in glass was increased by

more than an order of magnitude. In addition, due to the cutting, the sides of the glass piece develop rough spots which promote crack formation and glass rupture.

Flexing experiments

For solar cells on flexible molybdenum substrates, the setup used is sketched in Fig. 2-11. Since Mo foil serves as an electrically conductive back contact in this configuration, the apparatus was constructed out of acrylic blocks. The cell is held between two pieces of acrylic on the right; the nylon screw on the left bends the cell as light is directed from above. A microscope slide positioned on top of the cell fixes the area of the substrate that is bent. J-V readings were taken at different deflections and the stress calculated from the measured deflection caused by the screw. Using again the standard elasticity theory, [54] one can write

$$\mathcal{P}_{//} = E_{\text{Cas}} \frac{3txy}{2l^3} \quad (2.22)$$

where l is the substrate length and other dimensions are introduced in Fig. 2-11.

While this type of solar cells does not have the limitations of their fragile glass superstrate counterparts, their efficiencies are usually substantially lower, possibly due to shunting and high back barrier. Both of these factors may reduce the influence of piezoelectricity in the device. In addition, after several bending cycles they tend to undergo inelastic changes probably due to film cracking.

2.3.2 Piezo-data

The squeezing setup was used to examine a number of different CdTe based samples, made by either sputtering or closed space sublimation, having different back contacts, and areas from ~ 0.1 to 1 cm^2 . Also, it was examined that CIGS samples deposited on 2 mm glass substrate by co-evaporation, with the chemical-bath-deposited CdS layer, as described in Refs. [8, 11] Different pressure applicators were used ranging from those that covered almost the entire contact area to pogo-pins acting on local spots.

The first published 'piezo-PV' data from ref [9] are shown in Fig (2-12). Here

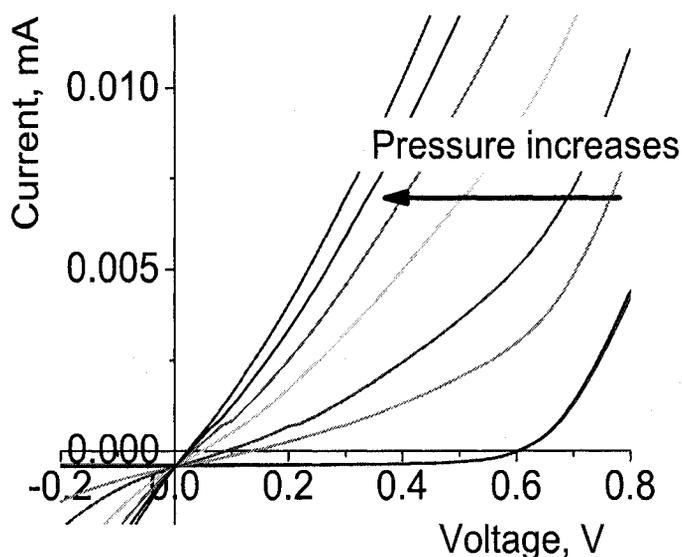


Figure 2-12: Pressure induced evolution of the current voltage characteristics of CdTe cells in squeezing experiments.

all the examined CdTe cells showed qualitatively similar strong piezo-response in IV

curves, illustrated in Figs. (2-13 and 2-14) for the illumination of about 0.01 sun. In all cases the effect was stronger for the case of small area applicators (pogo-pins), pointing at the pressure (and not the force) as a primary factor.

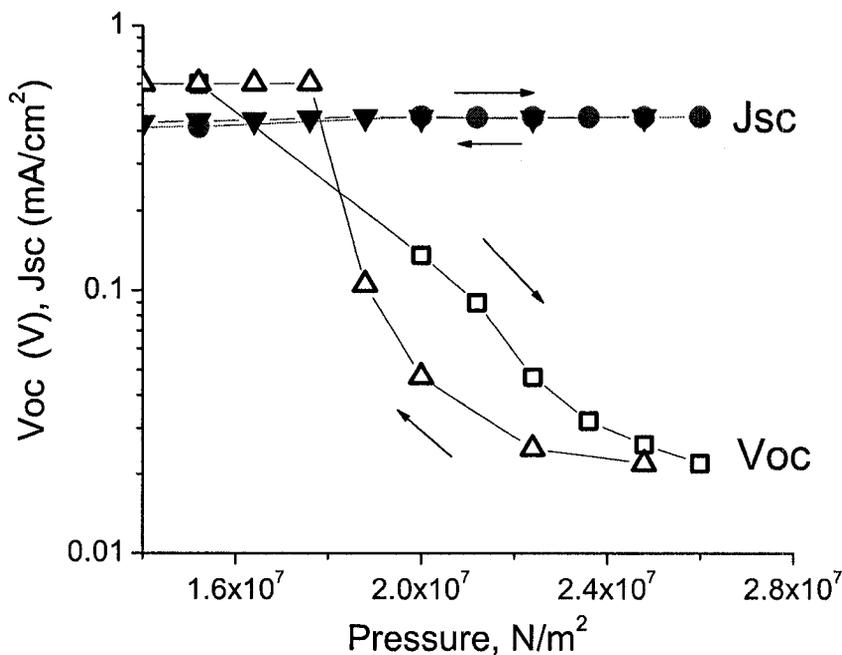


Figure 2-13: Open circuit voltage (V_{oc}) and short circuit current (J_{sc}) of the CdTe/CdS solar cell versus pressure. Arrows show the directions of pressure change.

The pressure induced changes appeared fully reversible allowing multiple cycling back and forth, although with a considerable hysteresis for some of the parameters, such as V_{oc} , similar to the pressure related hysteresis in polycrystalline film CdS resistance observed in Ref. [27]

The effect was found to start at higher pressures when the light intensity increased towards one sun, however retaining the amplitude from the original to almost zero V_{oc} . The observed logarithmically weak dependence of the threshold pressure \mathcal{P}_c on light intensity was consistent with the predictions in Eqs. (2.16) and (2.19).

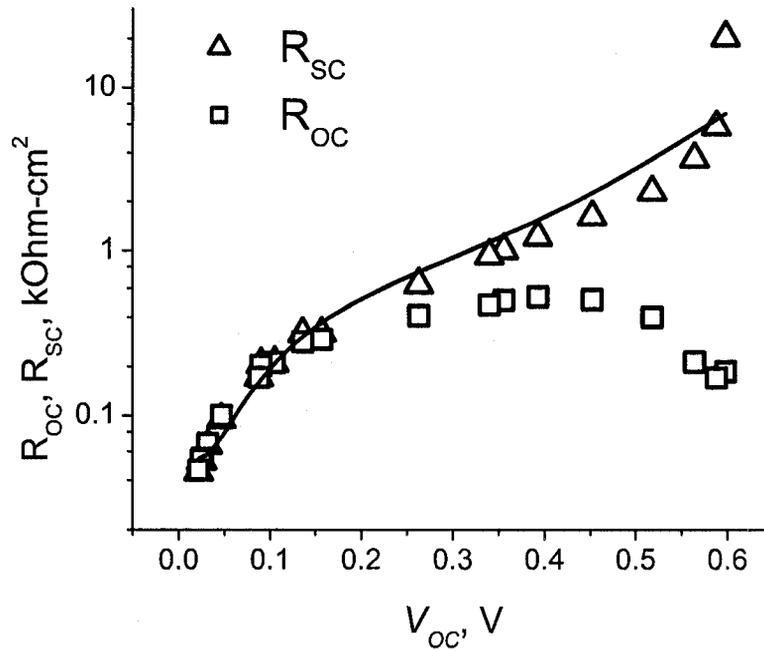


Figure 2-14: Short circuit (R_{sc}) and open-circuit (R_s) resistance vs. device V_{oc} driven by the external pressure. The dependencies include both the pressure up and down sweep data points showing almost no hysteresis in this format. The curve shows a fit of R_{sc} by Eq. (2.25) where R_s is given by the data.

From the current-voltage (J/V) curves corresponding to different pressures, we have extracted the standard set of PV parameters: V_{oc} , short-circuit current J_{Ssc} , shunt resistance R_{sc} , and series resistance R_{oc} . As plotted against V_{oc} (Fig. 2-14) the above PV parameters showed almost no hysteresis, pointing to a well defined electronic structure corresponding to each particular pressure.

It was verified that the pressure dependent parameters are observed in the CdTe cells with different thicknesses of the CdS and CdTe layers as illustrated in Fig. 2-15.

Shown in Fig. 2-16 is a set of data obtained in the squeezing experiments on CIGS samples. While the reversible piezo-effect is seen for both the voltage and current,

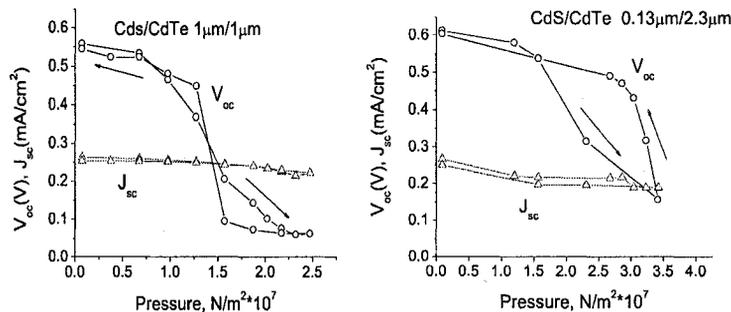


Figure 2-15: Open circuit voltage (V_{OC}) and short circuit current (J_{SC}) of the CdTe/CdS solar cell versus pressure. Arrows show the directions of pressure change.

its magnitude is much lower than that of CdTe cells in the above. This can be partially due to a thinness of CdS layer (at least three times thinner than those of our CdTe devices) and the substrate cell configuration leading to substantial shadowing as explained in the above Sec. 2.3.1. When the device on a glass superstrate is bent with

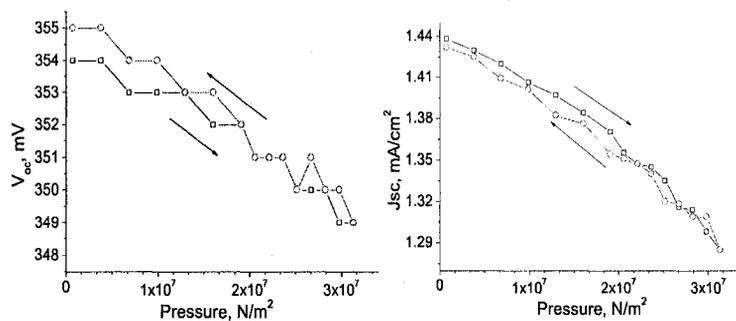


Figure 2-16: Open circuit voltage (V_{OC}) and short circuit current (J_{SC}) of the CIGS solar cell versus pressure. Arrows show the directions of pressure change.

film (cell) side up, as in Fig. 2-10, the CdS layer becomes stretched, developing stress similar to the case of pressure applied in direction perpendicular to the film surface.

For this arrangement it is observed the same trend as in our previous experiment.

Fig. 2-17 shows typical data for this configuration including a reversible decrease in V_{oc} and relatively small increase in J_{sc} with increasing stress.

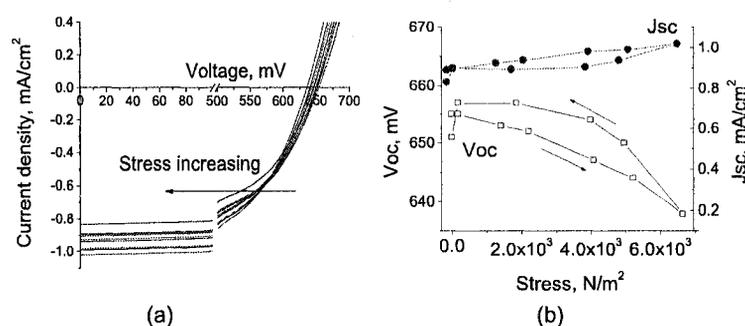


Figure 2-17: (a) Pressure induced evolution of the current voltage characteristics of CdTe cells in bending experiments. (b) Open circuit voltage (V_{oc}) and short circuit current (J_{sc}) of the CdTe/CdS solar cell versus pressure in bending experiments. Arrows show the directions of pressure change.

It was expected that when the film faces down and therefore is laterally in the course of bending, its V_{oc} might increase. Unfortunately, in the film-side-down configuration experiments the glass superstrates broke even easier and cells did not show the expected effect of the V_{oc} increase, opposite to what had been observed in the stretched (film-side-up) cells. In fact, in most cases, the glass broke before any noticeable change in PV parameters were observed.

Solar cells on flexible molybdenum substrates with the film side (contacts) up showed similar changes in V_{oc} and J_{sc} as those cells on glass. J-V data were acquired for complete cycles at three different light intensities, 0.02, 0.2, and 1 sun. Figs. 2-18 and 2-19 show J-V curves measured under 0.02 sun light intensity for increasing stress and the resulting stress dependencies for V_{oc} and J_{sc} . As with cells on glass, the effect

is more pronounced with lower light intensity. In particular, V_{oc} decreased as a result of bending by 4.8% at 1 sun, 7.2% at 0.2 sun, and 9.3% at 0.02. This dependence on light intensity may be due to partial piezo-effect screening by the photo-generated carriers.

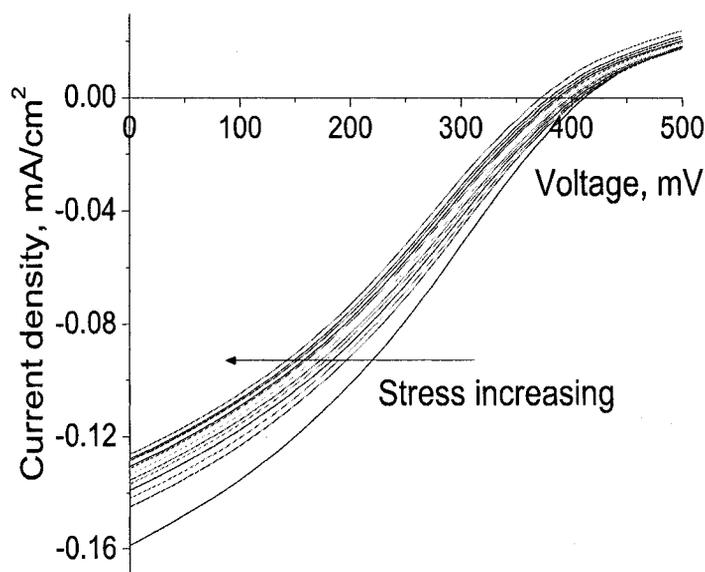


Figure 2-18: Stress-induced evolution of current-voltage characteristics of CdTe cells on flexible substrates.

While solar cells on flexible substrates represent the most convenient subject for our bending studies, their efficiencies are substantially lower, possibly due to shunting and high back barrier. As was mentioned before, these factors may reduce the influence of piezoelectricity on PV parameters of the device. In addition, after several bending cycles they tend to undergo inelastic fatigue probably due to film cracking. Remarkably, on fresh cells we have observed *increase* in V_{oc} under stress in the direc-

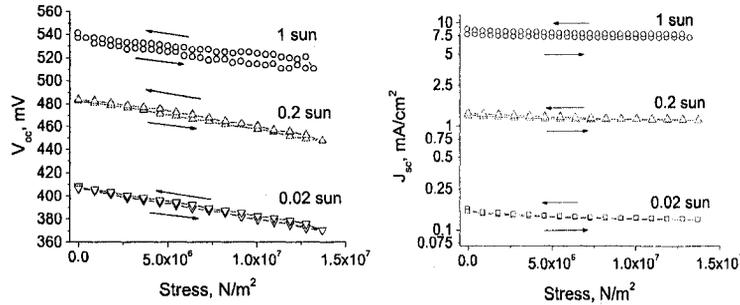


Figure 2-19: Stress-induced evolution of open-circuit voltage (V_{oc}) and short-circuit current (J_{sc}) of CdTe cells on flexible substrates under different light intensities.

tion of CdS film compression, but this effect became almost undetectable after several flexing sequences, which we attribute to a specific fatigue related to the film cracking.

2.3.3 Other related experiments

CdS occurs in two different crystal structures: hexagonal (wurtzite) and cubic (zinc-blend), depending on growth conditions, substrate, etc., of which only the former phase shows piezoelectric properties. Usually, thin films grow as a mixture of both phases, often with one phase being predominant. A major complication in exact phase ratio determination comes from the fact that some of the peaks of cubic and hexagonal structures overlap in XRD spectrum. In addition, since CdS is grown on TCO (SnO_2 in the case of CdTe-based superstrate cells), some of TCO peaks also overlap the CdS XRD spectrum. To overcome the intrusion of TCO signal and ensure that the structure does not change with thickness we prepared samples with three different thickness of CdS, 0.13 (standard), 0.4 and 1 μm .

The objective was to characterize crystal structure of CdS after it undergoes all processing steps of device fabrication, therefore we prepared fully functional CdTe solar cells of the type shown in Fig. 2-1(a) and verified the efficiencies for all three thickness of CdS layer. To expose CdS layer for XRD measurements, we etched CdTe layer off with a saturated solution of potassium dichromate in sulfuric acid. XRD spectra obtained for TCO as well as CdS of different thickness over TCO are shown in Fig. 2-20. While due to peak overlapping we cannot rule out the presence of cubic phase, we did not see any peaks corresponding solely to the cubic phase. At the same time several purely hexagonal peaks are clearly visible, especially in a thickest CdS sample. Additionally, except for expected signal enhancement, we did not find any noticeable change in crystal structure related to increase in film thickness. It can be concluded that in a working device CdS layer has predominantly hexagonal, i. e. piezo-active, crystal structure with preferential orientation along c-axis (002 plane in XRD data).

Also, the external electric field was attempted during the CdCl₂ treatment in order to additionally change the CdS grain dipole orientations (Fig. 2-21). To apply bias without blocking the oxygen, essential for successful treatment, from the CdTe surface, a wire mesh was used as a temporary 'back' electrode. The main problem with such treatments was that under high temperature (~ 370 °C) the structure transversal resistance was rather low resulting in significant shunting current. Furthermore, this effect was time dependent because the cell parameters evolved in the course of treatment. The present work was not able to solve these problems; hence, rather mixed results are presented in Table 2.1 with some indication of a positive

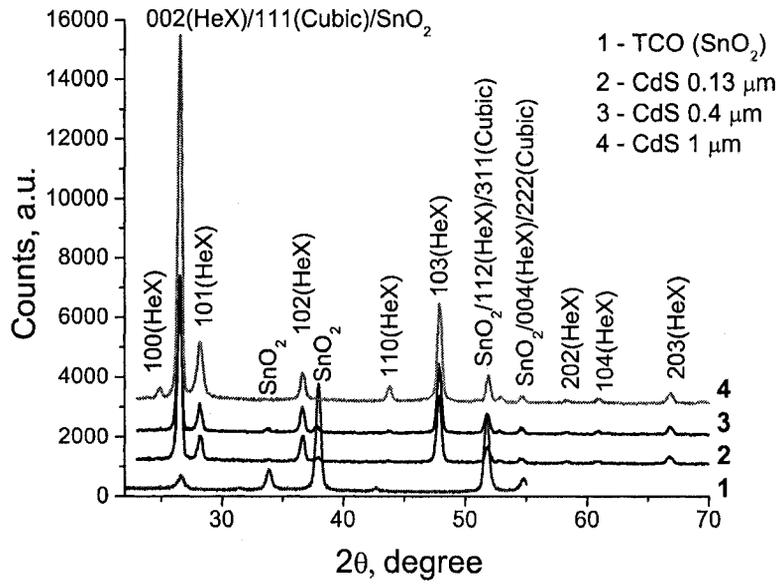


Figure 2-20: X-ray diffraction spectra of CdS/CdTe solar cell deposited on TCO for three different CdS layer thicknesses.

Parameter	OC	F, +6 V	R, -6 V	SC
V_{oc} , V	0.8 ± 0.05	0.77 ± 0.02	0.73 ± 0.04	0.73 ± 0.02
J_{sc} , mA/cm ²	20.5 ± 0.4	21.2 ± 0.6	19.9 ± 0.6	20 ± 0.5
FF, %	60 ± 4	63 ± 2	63 ± 3	63 ± 2
Eff, %	9.8 ± 1	10.3 ± 0.4	9.2 ± 0.8	9.8 ± 2.1

Table 2.1: PV parameters of CdTe cells after CdCl₂ treatment under the open-circuit (OC), forward bias (F), reverse bias (R), and short circuit (SC) conditions. Averages over 40 nominally identical cells for each condition.

effect due to the forward bias.

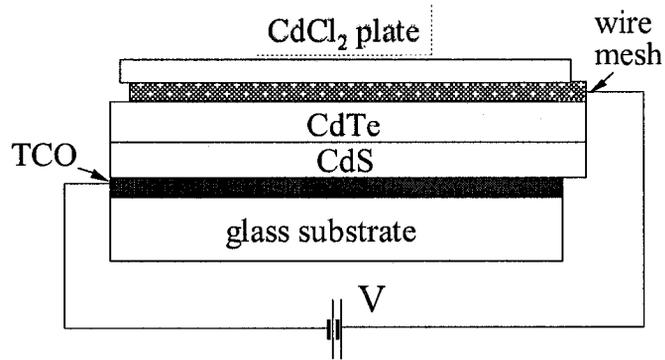


Figure 2-21: Design of the experiment for CdCl₂ treatment of CdTe cells under external electric bias.

2.4 Device operations & Model

This section discusses the effects of CdS electric polarization on device operation. We consider the polarization of both signs (i.e. leading to the above described 'gull-wing' shaped potential and the opposite one) in comparison with the 'reference' (traditional) device structure that does not have a dipole layer. The detailed analysis based on AMPS modelling was provided by M. L. C. Cooray and as described in the appendix A1 [59]. The main result is shown in Fig. 2-22. From the technological perspective, the range of positive fields ('gull-wing' region) in Fig. 2-22 is more attractive, since the PV parameters there are relatively independent of the CdS field strength and at the same time are relatively high corresponding to the experimental observed values.

One observation made in the course of modeling should be emphasized here: the polarization 'gull-wing' model turns out to be relatively independent on the underlying material quality (defect concentrations, mobilities, thickness), as opposed

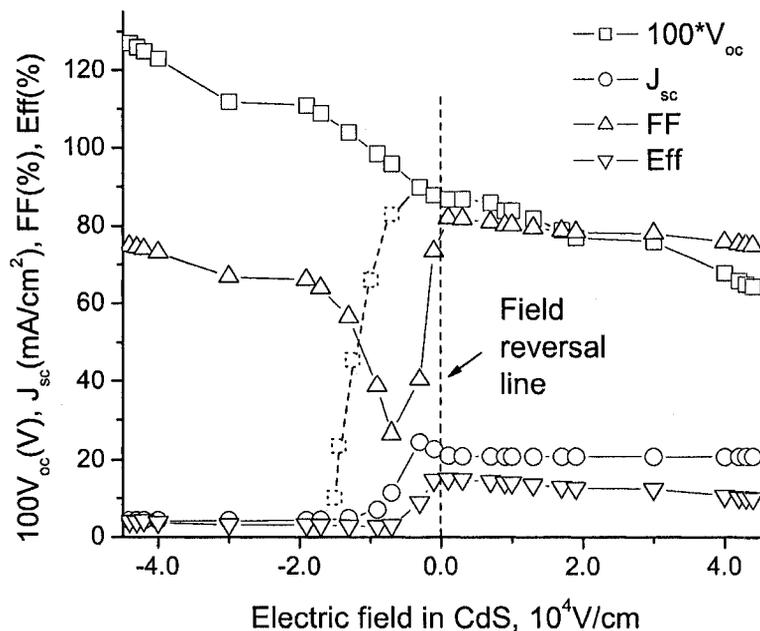


Figure 2-22: Open circuit voltage (V_{oc}), short circuit current (J_{sc}), fill factor (FF), and efficiency (Eff) vs. polarization electric field strength E . Positive field region corresponds to the case of polarization shown in Fig 2-6, Fig 2-7, called 'gull-wing model' [59]. The dashed branch of the V_{oc} curve corresponds to the shunting current cutoff beyond the AMPS modeling capabilities.

to the standard p-n junction models, for which the corresponding dependencies are extremely strong. Such a remarkable insensitivity of the "gull-wing" model has a simple physical explanation. Since the polarization electrostatic barrier in CdS turns out to be strong enough, it alone suffices to control the photovoltaic performance of the cell: adding defects and varying other parameters has only a minor effect on its operation. This differs qualitatively from the standard model, for which the material quality remains the critically limiting factor.

From the experimental perspective, the predicted properties of the 'gull-wing' model seems to be adequate: the devices made by different technologies in different

labs and from different source materials show surprisingly comparable parameters.

This is in agreement with the 'gull- wing' model predictions.

2.5 Discussion

The typical JV curves in Fig. 2-12, exhibit shape and evolution which, at the first glance, look shunt driven because of the drastic decrease in the short-circuit resistance R_{sc} (i. e. increase in the $J(V)$ slope at $V = 0$) with pressure. We argue that not only is this reversible behavior unrelated to shunting, but it proves rather the opposite, i.e. that shunting is insignificant.

Consider a well-known phenomenological equation of non-ideal photodiode [56] of any device model

$$J = J_0 \{ \exp[q(V - JR_s)/kTA] - 1 \} - J_L + V/R_p \quad (2.23)$$

where R_s and R_p are respectively series and parallel resistances, A is the diode ideality factor, and other parameters have their standard meaning. Under the standard condition $J_L \gg J_0$, and assuming that shunting is not severe, $R_p \gg V_{oc}/J_0$ (which is certainly the case for low pressures), one can derive the standard relation

$$V_{oc} \approx (kTA/q) \ln(J_L/J_0). \quad (2.24)$$

Furthermore, expressing from Eq. (2.23) the resistance $R = (dJ/dV)^{-1}$ leads to the following measurable short-circuit and open circuit resistances:

$$R_{sc} = \frac{R_s + R_L \exp[q(V_{oc} - J_L R_s)/kTA]}{1 + (R_L/R_p) \exp[q(V_{oc} - J_L R_s)/kTA]}, \quad (2.25)$$

$$R_{oc} = \frac{R_s + R_L}{1 + R_L/R_p}, \quad R_L \equiv \frac{kTA}{qJ_L} \quad (2.26)$$

where $R_L \sim 50 \text{ Ohm/cm}^2$ in the range of parameters corresponding to the data in Figs. 2-12, 2-13, and 2-14.

The pressure dependent resistances in Fig. 2-14 can now be explained by noting that Eq. (2.25) predicts indeed $R_{oc} \approx R_{sc} \approx R_s$ in the very low V_{oc} region where the exponential terms can be neglected. In that region the dependence $R_s(p)$ can be due to material parameters, such as pressure dependent band gap or the back barrier (beyond the present framework). This consideration predicts a noticeable deviation between R_{sh} and R_s for $V_{oc} \gtrsim 0.1V$, as observed, when the exponential term in the numerator becomes significant, while it remains immaterial in the denominator due to the large value of R_p . The corresponding fit in Fig. 2-14 is qualitatively consistent with the data. Moreover, the fact that R_{sh} exhibits a strong V_{oc} dependence in the high V_{oc} region means that the exponential term in the denominator of Eq. (2.25) is still insignificant; hence, large $R_p \gg R_L \exp(qV_{oc}/kT)$ testifying against shunting.

On average, the normal pressure induced changes correspond to the derivative $dV_{oc}/dP \sim 3 \cdot 10^{-8} \text{ Vm}^2/\text{N}$, which is consistent with $dV_{oc}/dT_j = d_{3j}/C_0$ with $d_{33} \approx 10^{-11} \text{ C/N}$, corresponding to the pressure along the c axis. [16] J_{sc} appeared the least sensitive showing $\lesssim 30\%$ changes attributable to pressure induced shift in the absorption edge [55] or other factors insignificant in what follows.

Finally, it is believed that the dramatic drop in V_{oc} observed in the squeezing experiments (Fig. 2-13 and similar) is consistent with the above developed understanding of CdS piezo-activity and device operations (Sec. A.1). Namely, the applied pressure gradually depolarizes the CdS grains changing the device band diagram from the (b)- to (c)-shape of Fig. A-1. When the applied pressure exceeds a certain value

the V_{oc} cut-off shown in Fig. 2-22 takes place in a relatively narrow pressure interval.

Relatively small pressure induced changes in CIGS parameters can be phenomenologically interrelated through Eq. (2.24), assuming the photocurrent change to be a cause,

$$\frac{\delta V_{oc}}{V_{oc}} = \frac{kTA}{V_{oc}} \frac{\delta J_L}{J_L}. \quad (2.27)$$

This is consistent with the measured $\delta J_L/J_L \sim 0.1$, $\delta V_{oc}/V_{oc} \sim 0.015$ and $kTA/V_{oc} \sim 0.15$. The observed $d(\ln J_L)/dp \sim 3 \text{ GPa}^{-1}$ is much higher than the pressure induced change in the band gap [57], $dG/dp \sim 0.05 \text{ GPa}^{-1}$. Therefore it cannot be attributed to the relative change in absorption. However, it can be readily explained within the the gull-wing singularity model of Fig. A-1 related to the pressure through the CdS barrier change as explained in Sec. A.1. Indeed, the pressure in our squeezing experiments was applied in such a way as to decrease the CdS barrier, thereby shifting the gull-wing singularity upward and *decreasing* the built in field in the CIGS layer. The latter decrease will impede the carrier collection, hence, decreasing J_L (note that $J_{sc} \approx J_L$ where J_L is generated in the CIGS layer, according to the 'gull-wing' model [49]).

More quantitatively, the upward shift in gull-wing singularity can be estimated based on Eq. (2.16) with $l \gg L$ and $\mathcal{P} \sim 10^7 \text{ Pa}$, $C_0 \sim 10^{-3} \text{ F/m}^2$, and $d_{33} \sim 10^{11} \text{ C/N}$, which gives $\delta V \sim 0.1 \text{ V}$. We then interpret the latter quantity as the effective forward bias applied to the device, which enables one to estimate the current change $\delta J_{sc} = J(\delta V) - J(0)$ relative to its short-circuit current $J(0) = J_{sc}$ based on the measured shape $J(V)$ of the device JV curve. This predicts $\delta J_{sc}/J_{sc} \sim 0.1$ consistent

with the observed effect.

The above explanation and estimates can be extended to the flexible substrate data in Figs. 2-18 and 2-19 that show the effect of similar magnitude and in the same pressure range.

Unfortunately, it was unable to explain along the same lines the bending experiment results in Fig. 2-17. The latter show almost as strong parameter changes under pressure that is about three orders of magnitude lower than that of CIGS squeezing and CdTe flexing experiments. We can speculate that either the abnormal glass fragility or unusual bending deformations affect some different variables, such as the cell back contact leading to the extremely strong pressure dependence that cannot be interpreted within the present framework.

In spite of the inconclusive results of our bending experiments, the squeezing and flexing experiments remain well explained by the CdS related piezo-electricity both qualitatively and semi-quantitatively. This interpretation is further confirmed by our XRD data showing a large fraction of the piezo-active hexagonal phase.

Two additional possible experimental verifications of the CdS piezo effect and dipole layer properties are called upon. (1) C-V measurements and analysis in light of the dipole screening length as explained in Sec. 2.2.3. In particular, a comparative study of C-V dependencies for different CdS thicknesses might be appropriate. (2) Using ultrasound to change the CdS voltage and modulate V_{oc} measured with a lock-in amplifier technique for different sound frequencies.

In spite of a limited success of our external bias treatment experiment (Sec. 2.3.3), it may open a new venue in device manufacturing, namely that of purposely applying

the electric bias and/or intense light in the course of structure deposition or postdeposition treatments. To the best of our knowledge, these directions have never been systematically explored.

One other new venue following from this work suggests a purposely created compression of CdS layer through its doping or deposition parameters (including elastically bent substrates), or tangent layer morphology. We note in this connection that Cu doping is known to strongly compress the CdS, [33] which may explain the known generally beneficial role of Cu doping [8] and the fact that it is not required for some kinds of substrates [58].

2.6 Conclusions

In conclusion, the following points of this chapter are considered to be most significant.

(1) CdS grains in thin polycrystalline films possess significant electric polarization and behave as electric dipoles. Their preferential orientation can be achieved either in the course of film deposition (frozen polarization) or as a result of high-temperature treatments (equilibrium polarization).

(2) The polarized CdS film creates a gull-wing shaped electric potential distribution with field reversal in the CdS region and its related electric potential drop $\lesssim 1$ V.

(3) The electrostatic screening of the CdS dipole layer is different from the standard Schottky length and depends on the layer polarization and thickness, which may

impact the interpretation of capacitance-voltage measurements.

(4) The gull-wing shaped electric potential distribution is generally beneficial for PV parameters making the technology rather forgiving with respect to variations in device and material parameters.

(5) Of the three experimental setups, the squeezing and the flexing results appear fully consistent with the strong piezo-effect in CdS. The bending setup results remain inconclusive due to the fragility of the glass substrates resulting from film depositions and treatments.

(6) The present work suggests new venues in PV technology, namely film deposition and treatments under external bias or light, and purposely created mechanical stresses in CdS through the deposition parameters, tangent layer morphology, or doping.

(7) The piezo - (pyro -) PV coupling explored in this work shades some light on the mechanisms of high-temperature (CdCl_2) postdeposition treatments and Cu-doping as affecting the CdS stress and polarization.

(8) New experimental verifications are suggested, including C-V measurements and ultrasound induced variations in V_{oc} .

In general, the above results call upon further work on piezo- (pyro-) PV coupling including both the experimental work and theoretical modeling.

Chapter 3

Fundamental drift of Parameters in Phase Change Memory

3.1 Introduction

Recently, phase transformations in chalcogenide materials [60] have attracted a great deal of attention [61] as the basis for the phase change memory (PCM) technology [62]. PCM devices utilize electrically initiated, reversible rapid amorphous-to-crystalline phase change in multi-component chalcogenides, such as $\text{Ge}_2\text{Sb}_2\text{Te}_5$ (GST). The markedly different crystalline and amorphous state resistances are used as the two logic states. The crystalline GST has two possible structures: a stable hexagonal structure and a meta-stable face centered cubic (FCC) lattice. The hexagonal structure is a high temperature phase, while the reversible transformations between cubic and amorphous is used for memory storage (see Fig 3-1) The metastable GST consists of two well-defined 3D repeat units:- Te-Ge-Te-Sb-Te- (I) and -Te-Sb-Te-Ge-

(II). The phase change from the cubic to hexagonal is the movement of unit II in the [210] direction (see Ab initio calculation [63]).

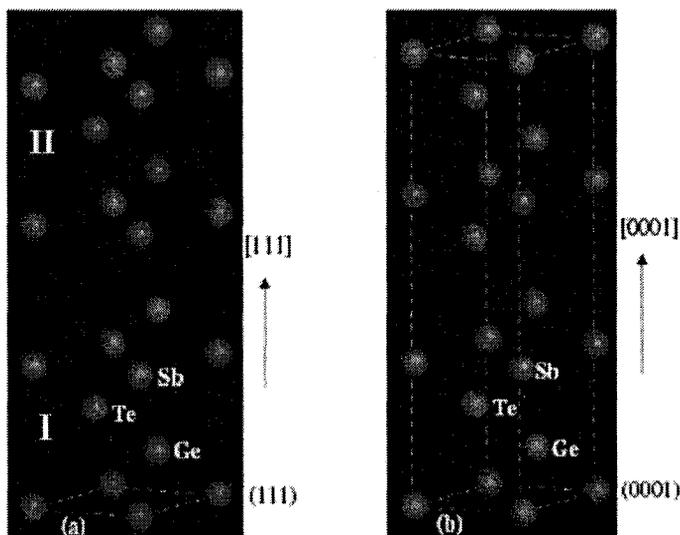


Figure 3-1: (a): Atomic arrangement of metastable $\text{Ge}_2\text{Sb}_2\text{Te}_5$ built based on (111) planes along the [111] direction. (b): Stable crystal structure of hexagonal $\text{Ge}_2\text{Sb}_2\text{Te}_5$.

We recall that, as illustrated in Fig. 3-3, the electric current ('reset') pulse through the crystalline (set) phase generates heat, which melts the material [64]. After the current is turned off, the melted portion rapidly cools down freezing in the two - three orders of magnitude more resistive amorphous ('reset') state. Fig. 3-2 shows different domains of the IV curve labelled with 1, 2, 3 and 4. Initially the domain 2 of the IV curves shows that the device is in the amorphous phase after the melted portion rapidly cools down freezing to a more resistive state with a resistance of 2 orders in magnitude or more. Then it switches (thresholds) to domain 3, low resistive state

when the voltage across the amorphous phase grows above the threshold value V_{th} . After the threshold event, the current rises more (post switching) shown in domain 4 with a resistance of 2 orders less than the domain 2 due to moderate current (set pulse) which generates additional heat that crystallizes the amorphous material and it is now in the conductive phase of domain 1 [62]. Fig. 3-3 shows a programming reset pulse followed by a read pulse of 0.2 v, to read the state of these devices and its value is much below the threshold voltage of the PCM devices.

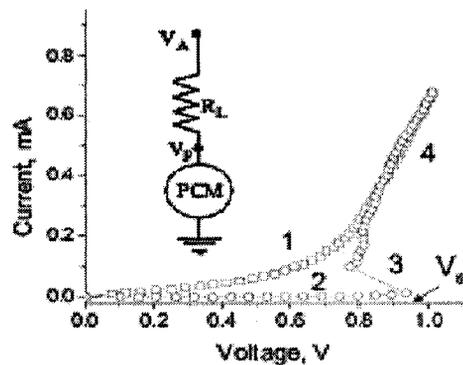


Figure 3-2: The typical PCM current-voltage (IV) characteristics include domains corresponding to: 1 - conductive phase, 2 - insulating phase, 3 - switching, 4 - post-switching. Shown on the inset is a sketch of the experimental setup. V_A and $V_P = V$ are respectively the applied and the probe measured voltages, whose differential determines the current (I) as divided by the load resistance (R_L).

The drift phenomena have important practical implications because they lead to spontaneous changes in the measurable device parameters (such as R) used for recording and reading the PCM information. This work relates the observed parameter drift to the inherent structural relaxations in a glass. This work points at the important

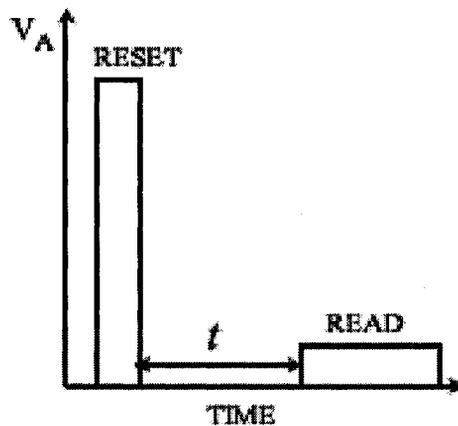


Figure 3-3: definition of the drift time t . The read voltage much lower than V_{th} allows measurements without causing any structural changes.

role of atomic dynamics in PCM operations.

3.2 Experimental

The basic measurement circuit for these experiments are explained in Fig. 3-4, where the Qbox (Intel's custom made delay circuit with amplifier and a load resistor) which basically controls the programmable current through the device. It is connected to the computer through DAC (Digital Analog Converter) interface card and is powered by a power supply. A pulse generator is connected to one of the input of the Qbox which basically supplies the electrical pulse to the device under test (DUT) and the other output of the Qbox is connected to an Oscilloscope which captures the output signal. There are metal probes which connects the DUT to the

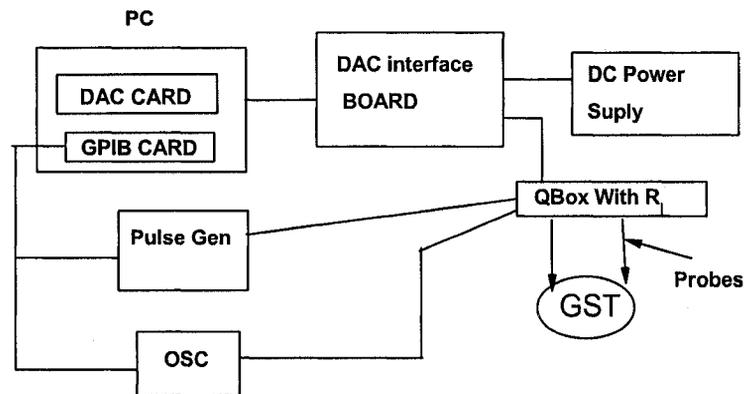


Figure 3-4: Basic Block diagram of the measurement circuit used to measure the Drift of $V_{th}(t)$ and R . General Purpose Interface Bus (GPIB), Digital Analog Converter (DAC) and Oscilloscope (OSC) were used in the circuit.

Qbox. The GST devices were made at Intel's Fab with the state of art technology (Intel Confidential). Basically the GST is deposited as amorphous between two metal electrodes, the top and bottom electrodes. After lithography and chemical mechanical polishing the patterned GST was exposed to the probes for electrical testing.

For the experiment of partially reset PCM cells, we have used Fig. 3-5. We apply a Reset pulse of certain amplitude (amplitude will vary depending upon how much we want to RESET them- 5v or 10v) , pulse width and then wait for time t_1 and t_2 and measure voltage at each of those intervals with a Trapezoidal read pulse of fixed width and amplitude.

The amorphous state appears in PCM upon fast cooling (quenching) of a melted portion of material created by passing a strong reset current pulse through the device. That portion occupies a finite volume (Fig. 3-6), which increases with reset voltage used to melt the material. When small enough, that volume depends on

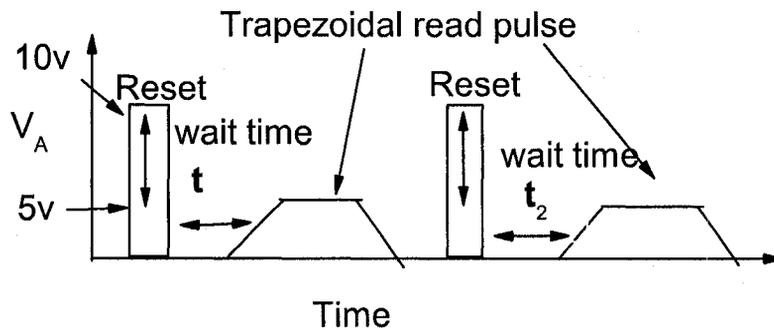


Figure 3-5: Drift $V_{th}(t)$ pulse measurement technique for different partially reset PCM cells.

reset voltage and so do its related resistance R and threshold voltage $V_{th}(t)$. This explains our observations in Fig. 3-6 where the threshold voltage and its drift exhibit 'programming voltage dependencies in such structures that are commonly referred to as partially reset. The reset voltage dependencies saturate when the the amorphous volume becomes large enough, after which the structure is referred to as fully reset. In particular, the full reset resistance R does not depend on the reset voltage or current. In the majority of the experiments, Intel's PCM cells fully reset to the resistance saturation level were used. However, the data on partially reset structures show almost no dependence on reset voltage as normalized to its initial value as illustrated in Fig. 3-7.

Our experimental setup and the definition of drift time are illustrated in Fig. 3-1. First the devices were RESET and then they were allowed to drift from $100\mu\text{s}$ to 10 ms and correspondingly the voltage was read at those intervals. 30 to 100 measurements were performed for each experimental point. A lower time boundary of 0.1

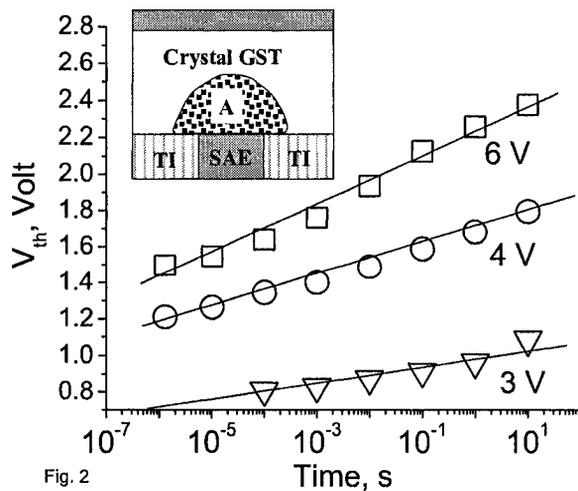


Figure 3-6: Drift $V_{th}(t)$ for three partially reset PCM cells, in which the amorphous region was created under different reset voltages shown next to the curves. The inset PCM sketch [64] shows the crystalline and amorphous (A) GST phases, the small area electrode (SAE) and thermal insulator (TI).

μs was chosen to avoid the post-melting temperature variation effects for $V_{th}(t)$ measurements, while it was limited by 1 s for $R(t)$ measurements due to the experimental conditions used. As suggested by the log-log slope in Fig. 3-8, the typical resistance data are approximated by the power dependence,

$$R(t) = R(t_0) (t/t_0)^\alpha \quad (3.1)$$

where t_0 is arbitrarily chosen zero time. α was in the range of 0.03 to 0.1 depending on the device type and degree of reset. Unlike $R(t)$, the linear slope $V_{th}[\log(t)]$ over almost 9 orders of magnitude in time, suggests the logarithmic dependence

$$\frac{\Delta V_{th}(t)}{V_{th}(t_0)} \equiv \frac{V_{th}(t) - V_{th}(t_0)}{V_{th}(t_0)} = v \ln \frac{t}{t_0}. \quad (3.2)$$

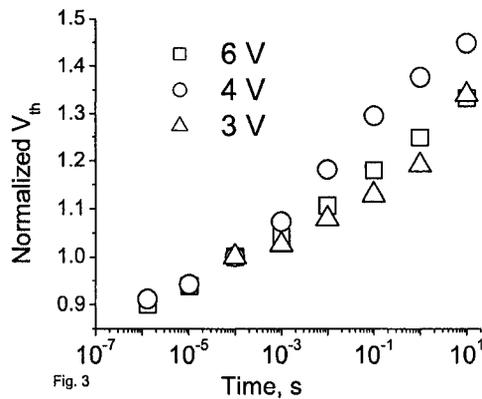


Figure 3-7: Drift $V_{th}(t)$ for three partially reset PCM cells, same as in Fig. 3-6, normalized to the absolute values of the corresponding voltages at 0.1 ms.

It is observed that $v \sim 0.02 - 0.04$ increases with temperature T (Fig. 3-11) and independent of thickness (Fig. 3-9, Fig. 3-10) using the pulse technique Fig.3-12 (where you basically heat the device and at that instant apply a Reset pulse of certain amplitude, pulse width and then wait for time t, t_2 and read with a trapezoidal pulse of fixed width and amplitude at those interval.).

It is known that the higher the thickness of GST, the higher is the $V_{th}(t)$ and this is verified by an experiment using Fig. 3-1 right, where different $V_{th}(t)$ were recorded for different GST thickness at certain time and plotted against thickness (Fig. 3-13). So threshold voltage $V_{th}(t)$ is linearly proportional to thickness of GST. The current voltage characteristic of these devices were measured for 2 thickness of GST 300\AA and 1000\AA at different wait times after they have been Reset and then allowed to drift (Fig. 3-14).

To study the ageing phenomena in glass a specially designed experiment was carried out, where the sample was at first well Reset and then annealed at 100°C and

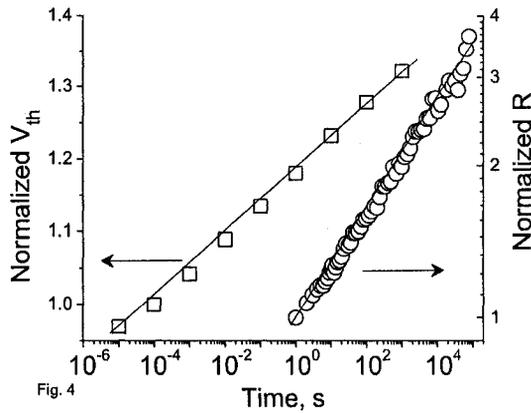


Figure 3-8: Temporal drift of $V_{th}(t)$ and $R(t)$ arbitrarily normalized to $t = 0.1$ ms and $t = 2$ s respectively. Note the logarithmic scale of the R -axis.

75c and then measured at room temperature (see Fig. 3-18). It was observed that the dependence $V_{th}(t)$ saturated at large time anneal at T well above room temperature (Fig. 3-16) and similar saturation of the resistance (Fig. 3-17).

Finally, we note that while the linear slopes in Fig. 3-8 appear most typical, data on devices of certain architecture exhibit a slight super-linearity better fit with a polynomial quadratic in $\log(t)$ (Figs. 3-7 and 3-11).

3.3 Phenomenological DWP model

While the author of this thesis took part in developing the physical understanding of the observed parameter drift, the formal part of the model was developed by V. G. Karpov and Y. A. Kryukov [92]. The observed drift can be related to the ageing phenomena, in the course of which a metastable glass structure relaxes to its more stable state [68, 69]. It is typical that such relaxations exhibit logarithmically

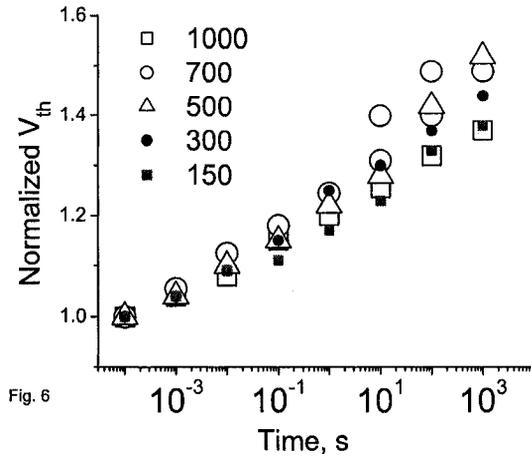


Figure 3-9: Drift of threshold voltage $V_{th}(t)$ normalized to the the corresponding initial values for fully reset samples of different thicknesses between 150Å and 1000Å.

slow temporal dependencies of the refractive index, sound velocity, etc., resembling that of the low temperature specific heat and related quantities [70]. The latter are phenomenologically described in the terms of random double well potentials (DWP) (Fig. 3-15) representing a metastable disordered atomic structure in a glass [71].

The DWP concept [71] accounts for a structural disorder (including bond angles, lengths, and coordination numbers), which makes some elements in a glass excessively flexible. Their atoms can move between two different configurations corresponding to the two energy minima in DWP (comparable transition rates between three or more configurations would appear a sheer coincidence in a random glass structure). Structural disorder translates into the fluctuations of DWP barrier height and energy difference. A simple commonly accepted hypothesis about their probabilistic distributions is that they are uniform within certain limits. This useful approximation is valid when the distribution widths are greater than the corresponding energy intervals

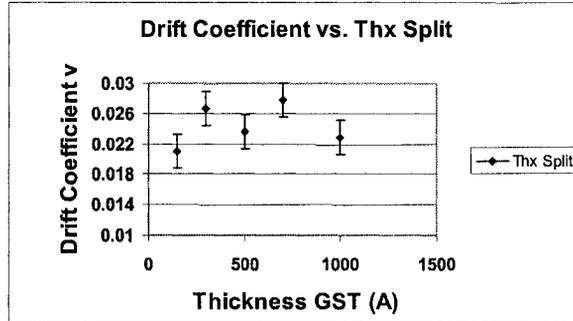


Figure 3-10: Drift coefficient of threshold voltage $V_{th}(t)$ vs. various Thickness of GST. Note that there is a 15 %-20 % variation in drift coefficient which can be due to experimental inaccuracy.

of experimental significance. While in reality these distributions may be not uniform and having continuously decaying tails, etc., the uniform approximation was shown to give at least semi-quantitative description of surprisingly wide variety of phenomena in practically all kinds of glasses [69–72]. While the microscopic nature of moving atoms can be different in different glasses, the phenomenological DWP model has become a commonly accepted universal concept of atomic dynamics in glasses.

The DWP concept introduces the exponentially broad distribution of relaxation times $\tau(W_B) = \tau_0 \exp(W_B/kT)$. Because the barrier height W_B is a random quantity with almost uniform probabilistic distribution

$$g(W_B) \approx 1/\Delta W_B, \quad \Delta W_B = W_{B,max} - W_{B,min} \quad (3.3)$$

between its boundary values, the maximum and minimum relaxation times in the

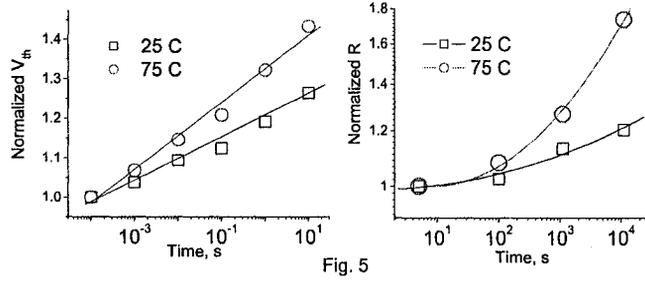


Figure 3-11: Drift $V_{th}(t)$ and $R(t)$ at two temperatures.

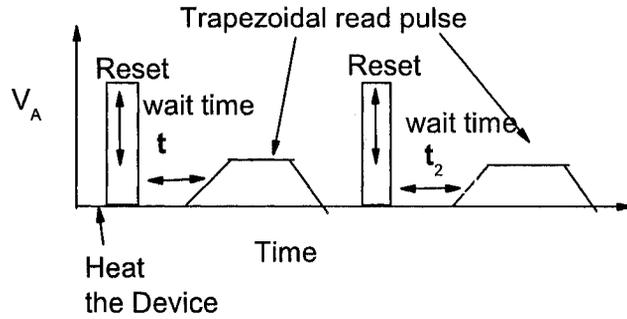


Figure 3-12: Pulse Measurement Technique for measuring Drift of $V_{th}(t)$ and $R(t)$ of PCM cells at two temperatures.

system are estimated as

$$\tau_{max(min)} = \tau_0 \exp(W_{B,max(min)}/kT). \quad (3.4)$$

The relaxation time distribution takes the form

$$\rho(\tau) = g(W_B) \left| \frac{dW_B}{d\tau} \right| = \frac{kT}{\tau \Delta W_B}, \quad \tau_{min} < \tau < \tau_{max}. \quad (3.5)$$

Integrating the latter distribution from τ_{min} to the time of the experiment t yields

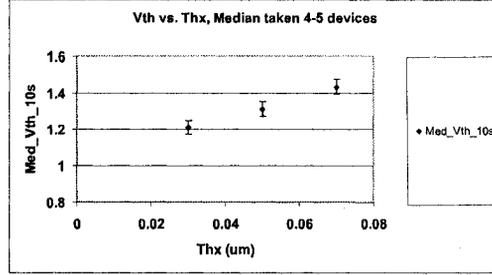


Figure 3-13: Threshold voltage $V_{th}(t)$ for fully reset samples of different thicknesses of 300Å, 500Å and 700Å.

the fraction of 'active' DWP

$$f(t) = \frac{kT}{\Delta W_B} \ln \left(\frac{t}{\tau_{min}} \right) \quad \text{when} \quad \tau_{min} < t < \tau_{max}. \quad (3.6)$$

$f(t)$ saturates at $f_{max} \equiv f(\tau_{max}) = 1$ for times $t > \tau_{max}$ and can describe a remarkably broad time interval ranging from τ_{min} shorter than one microsecond to, say, $\tau_{max} \sim 10^5$ s assuming $\tau_0 \sim 10^{-13}$ s (characteristic atomic vibration time) and $W_{B,max} = 1$ eV as a rough guide estimate. If a physical quantity, such as the material density, stress, etc. changes with f insignificantly, then its f -dependence can be linearized, which, according to Eq. (3.6) predicts logarithmically weak temporal dependencies.

A simple assumption specifying the above phenomenology is that f is proportional to the relative volume change (dilation),

$$u(t) = u_0 f(t), \quad (3.7)$$

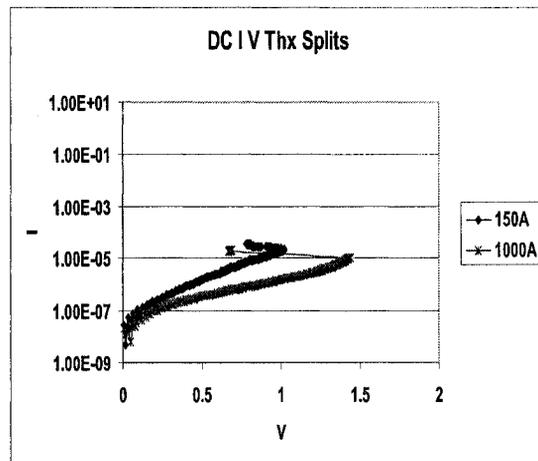


Figure 3-14: IV characteristics of a typical GST material measured at Intel Lab showing that higher thickness of GST has higher threshold voltage. In this case 1000\AA has V_{th} of 1.5v and 150\AA has V_{th} of 1v.

which affects the observed quantities V_{th} and R . Here u_0 is the ultimate dilation after $t > \tau_{max}$. Based on the available data [68] we assume the order of magnitude estimate $|u_0| \sim 0.01$.

Indeed, it has been long known [69, 73, 74] that hydrostatic pressure, hence, the dilation affects the electric and atomic characteristics of glasses, which relax logarithmically in time after the pressure application or removal. In a PCM structure, a strong internal pressure builds at the reset stage due to a considerable difference (of several percent) between the specific volumes of the crystalline phase and the melt. Its subsequent freezing will then create a compressed amorphous dome (Fig. 3-7) whose dilation will tend to increase over time, consistent with the stress relaxation data [75].

The resistance change is related to u through the activation conduction in the

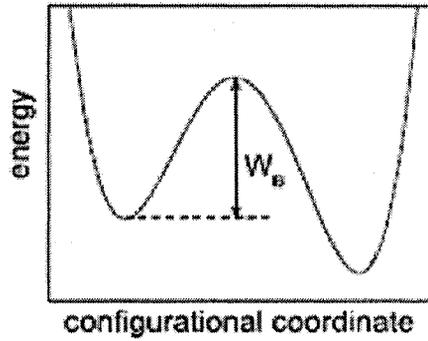


Figure 3-15: Double well atomic potential (DWP) with the barrier height W_B .

form,

$$R \propto \exp(E_F/kT) \quad (3.8)$$

typical of chalcogenide glasses [60]. In the standard approximation, the energy gap E_F between the Fermi level and the mobility edge depends on u linearly,

$$dE_F/du = D,$$

where the deformation potential D is typically positive, and is in the range of $D \sim 1-3$ eV. [73, 76, 88] Combining Eqs. (3.6) - (3.8) yields the dependence in Eq. (3.1) with

$$\alpha = u_0 D / \Delta W_B. \quad (3.9)$$

Assuming for numerical estimates $\Delta W_B \sim 1$ eV, $D/\Delta W_B \sim 1-3$ and $u_0 \sim 0.01$ predicts $\alpha \sim 0.03$ of the order of the observed values. As opposed to the former case,

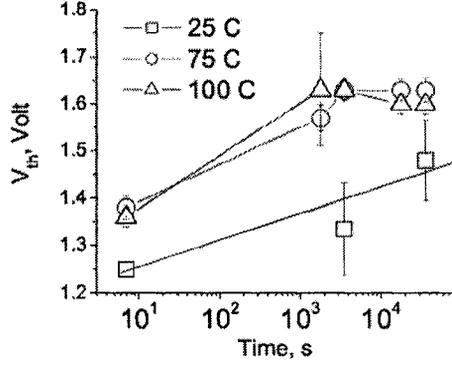


Figure 3-16: Saturation of $V_{th}(t)$ after high temperature anneal vs. lack of saturation at room temperature. All the data were read at 25 C.

$V_{th}(t)$ is not activated and therefore is described in the linear approximation,

$$V_{th}(t) = V_{th}[u(t)] = V_{th}(0)[1 + \beta f(t)]. \quad (3.10)$$

In the current phenomenological framework, $\beta \equiv [\partial \ln(V_{th})/\partial f]_0$ remains a dimensionless material parameter. Substituting here Eq. (3.6) yields Eq. (3.2) with

$$v = \beta kT/\Delta W_B \quad (3.11)$$

Using $\Delta W_B \sim 1$ eV, $kT \sim 0.025$ eV, and $\beta \sim 1$ predicts $v \sim 0.025$ consistent with the observations. We conclude that DWP model correctly describes the observed drift phenomena including the numerical values of parameters. It predicts the drift saturation for $t \gtrsim \tau_{max}$. Estimating $\tau_{max} \sim 10^4$ s from Fig. 3-16 (a) predicts the maximum DWP barrier $W_{B,max} = kT \ln(\tau_{max}/\tau_0) \approx 1.2$ eV (in the range of expected

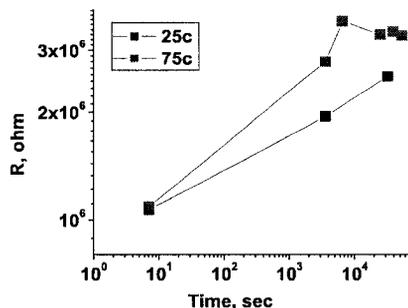
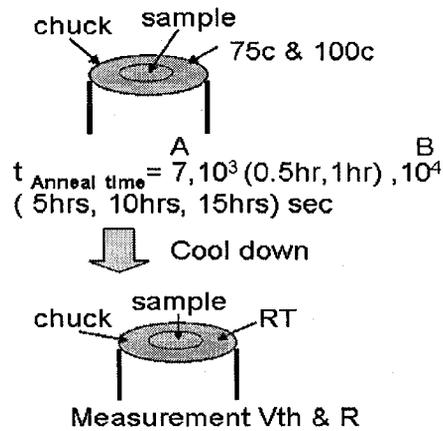


Figure 3-17: Saturation behavior of R at 75c compared to no saturation behavior of R at 25c.

values) and the room temperature saturation at $t \sim 10^7$ s. Variations of ΔW_B , $W_{B,max}$ and D between different glasses will have a strong impact on the drift phenomena, which in some cases may become suppressed. A universality of the DWP concept is clearly seen from the data in Fig. 3-7 showing that glass structures created under different 'reset' voltages, exhibit very similar V_{th} drift patterns when normalized in accordance with Eq. (3.10). The interpretation in Eqs. (3.10) and (B.9) relates the slopes

$$d \ln(V_{th}) / d \ln(t) = v$$

in Fig. 3-7 to the barrier distribution widths ΔW_B , which are apparently not very different between differently reset samples. In addition, we note that the above thickness-independent expression for the drift coefficient v is fully consistent with our data in Fig. 3-9. The observed super-linearity of V_{th} vs. $\log(t)$ can originate from a nonuniform distribution $g(W_B)$ and/or from the higher degree of disorder in the 'not-fully-reset' devices where the remnant crystalline inclusions make the frozen



Expect saturation at certain Anneal time
 When glass reaches equilibrium.

Figure 3-18: Experimental set up to study the saturation behavior of V_{th} (anneal time) and R (anneal time). The PCM devices (sample) were initially heated in the chuck to the desired temperature of 75c or 100c for those annealed times, mentioned in the plot. Then they were measured at room temperature after cooling.

dome a two phase system. It was shown indeed [69] that relaxations quadratic in $T \log(t)$ take place when, in addition to W_B , other DWP parameters are significantly dispersed. Using fits linear in $T \log(t)$ will then make the estimated α and v/T increase with T , which could explain some of our observations.

It follows from the above analysis that the observed drift phenomena are correctly predicted by the DWP concept describing long-time relaxations in the atomic system of a glass.

3.4 Discussion

The conclusion that the drift of glass parameters in PCM devices can be related to atomic dynamics in DWP, can have a broader significance for the physics of glasses. First, it establishes a tool set for tracking relaxations of atomic glass structure during very long time intervals at room and higher temperatures; the previous long time relaxation experiments were limited mostly to specific heat at extremely low $T \sim 1 - 10$ K, since non-DWP contributions masked the effect at higher temperatures [70]. Secondly, the PCM created amorphous material at nano-scale exhibiting the same DWP dynamics as virtually all other glasses, gives a unique proof of universality of glass properties down to very tiny space scales. Thirdly, detecting the known DWP glass properties entails other DWP related predictions, such as the presence of soft atomic potentials (extending the DWP model over higher energy region) abnormal polaron effect, negative correlation energy, etc. (see *e. g.* the review by Galperin *et al.* in Ref. [70]), to be scaled down to nano materials, possibly paving a way to an interesting overlap between the physics of glasses and nano-technology.

Earlier work in Ref. [78] mentioned too the possibility that mechanical stress release could underly the PCM parameter drift. While somewhat similar to our present understanding, that work did not relate the observed drift to the DWP dynamics and, therefore, no analytical equations for $R(t)$ and $V_{th}(t)$ were derived. Furthermore, the authors [78] eventually argued against the stress relaxation hypothesis in favor of an 'electronic' explanation based on certain interpretation of their interesting experiments that we discuss next.

In the course of these experiments, [78] (i) the 'electronic switching' from reset to the conductive set state was achieved by forcing relatively low current pulses, insufficient to melt the material. However, (ii) so achieved switched (set) state was not long leaved enough recovering back to the amorphous (reset) state, and (iii) the 'reinstated' resistive state exhibited the same drift as observed before switching.

The latter observations were interpreted as testifying against the stress relaxation mechanism (and in favor of 'electronic' explanation) because "...the microscopic mechanisms responsible for drift are fully reversible with respect to electronic switching even if no phase transition takes place" [78].

However the above outlined experiments can be interpreted without references to electronic mechanisms. A 'non-electronic' interpretation is readily offered by the nucleation switching model [67,79]. We conclude that the experimental results of Ref. [78] do not require 'electronic' mechanisms to be explained and are fully consistent with both the atomistic models of switching [79] and drift.

3.5 Conclusions

In summary, a significant additional data on drift dynamics of PCM parameters was obtained and demonstrated how the classical double well potential concept explains the entire data. More specifically, we point at the following findings in this work.

- (1) The drift observation range extended to almost nine decades in time.
- (2) Normalized drift $V_{th}(t)$ in partially reset PCM cells does not depend on reset

voltage and has the drift coefficient v that depends only on glass parameters.

(3) V_{th} drift coefficient v increases with temperature, but does not depend on device thickness.

(4) The drift saturates for both V_{th} and R at long enough time, which is $\sim 10^4$ s at $T = 75$ C and is predicted to be $\sim 10^7$ s at room temperature.

(5) The available data on drift dynamics, both here and previously published are fully consistent with the classical double-well-potential model, which gives simple analytical expressions for the observed temporal dependencies including numerical parameters.

Chapter 4

Field Induced Nucleation in Phase Change Memory

4.1 Introduction

The recent development in chalcogenide phase change memory (PCM) [81], revived interest in physics of crystal nucleation and glasses and its related phenomenon of switching. We recall that PCM utilize electrically initiated, reversible amorphous-to-crystalline phase changes in multi-component chalcogenides, such as $\text{Ge}_2\text{Sb}_2\text{Te}_5$ (GST); the markedly different phase resistances are used as the two logic states. Switching from the high-to-low resistive (crystalline) state is triggered by voltages exceeding certain threshold value V_{th} . Physically, switching creates a cylinder-like crystalline inclusion shunting through the amorphous host.

Switching in chalcogenide glasses was originally introduced by Ovshinsky [82] who suggested that it "...can be analyzed in terms of nucleation theory wherein the

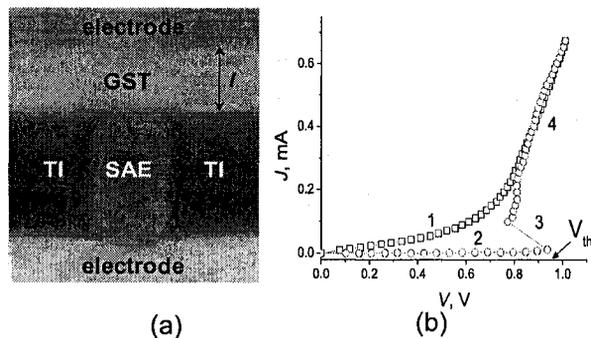


Figure 4-1: (a) TEM image of a functional part of the Intel fabricated PCM: SAE is the small area electrode and TI is the thermally insulating dielectric. The switching process results in a conductive crystalline filament between SAE and top electrode. (b) Typical PCM IV characteristics: 1 - conductive (crystalline) phase IV, 2 - insulating (amorphous) phase IV, 3 - switching portion, 4 - portion of IV following the threshold switching.

nucleation rate is dependent on the applied voltage” and even announced the corresponding model ”to be published”. However such a model was not developed until very recently [83].

The nucleation switching concept states that in a strong enough field nucleation evolves through the barriers that are substantially lower than the standard nucleation and consistent with the observed switching times. New phenomenon of *under threshold* switching is discovered in this work, in contrast with the standard threshold switching (above V_{th}).

4.2 Model

The resistive state of PCM is represented by a flat plate capacitor filled with an amorphous material of high resistivity. The nucleation switching in high electric field

starts with a cylinder shaped conductive crystal embryo (see Fig. 4-2) which concentrates the electric field at its end, which then facilitates nucleation of additional particles at its end, further increasing its length, the field strength, etc. This instability leads to a low resistive crystalline filament shunting across the structure. The embryo induction time $\tau = \tau_0 \exp(W/kT)$ is interpreted as the switching delay time (between the voltage application and the switching event). On experimental grounds, it must be short enough (say, $\tau \lesssim 10^{-7}$ s), thus requiring a rather low nucleation barrier W .

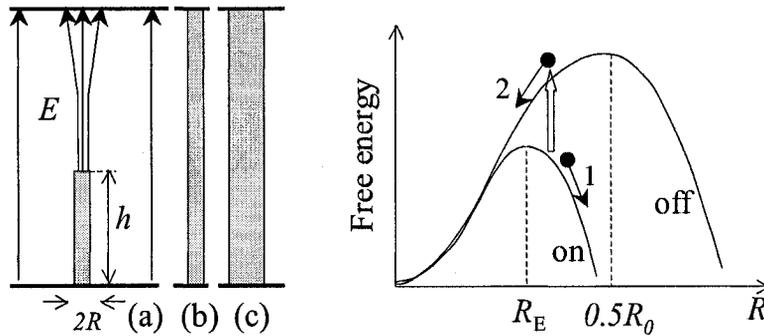


Figure 4-2: Left: evolution of the filament embryo through its primary nucleation (a), secondary nucleation events (b), and radial growth (c): arrows represent the electric field lines. Right: the free energy of the crystalline filament vs. its radius for the cases of on and off electric field. Arrows 1 and 2 represent respectively the filament radial growth and decay when the field is off (fat arrow).

The field induced nucleation was noticed earlier for glassy materials in moderate fields [66], much below the typical switching fields in PCM. Its mechanism is a strong polarization of a new phase particle that reduces the electrostatic energy. This effect is much stronger in a filament embryo due the 'lightning rod' type of field enhancement [79], by $\sim (h/R)^2 \gg 1$ where h and R are respectively the embryo length and radius.

Strong electric field facilitates nucleation of additional particles at the embryo end, shunting the structure (Fig. 4-2).

More quantitatively, the filament embryo free energy is $F_f(R, h) = 2\pi Rh\sigma - \pi R^2 h\mu - h^3 E_0^2 \varepsilon / 8$ where σ and μ are respectively the surface tension and the chemical potential difference between the two phases, ε is the dielectric permittivity of the host material, and the third term accounting for the electrostatic energy. A straightforward analysis of $F_f(R, h)$ (to be published elsewhere [97, 98]) shows that the nucleation favors small R , so that the minimum barrier $W_{min} \equiv W$ corresponds to the minimum possible radius R_{min} of a continuous crystalline cylinder in a glass host. Denoting $R_{min} \equiv \alpha R_0$, the parameter α is typically in the range of $0.1 \lesssim \alpha < 0.5$ where $R_0 = 2\sigma/\mu$ is the classical nucleation radius; here $\alpha = 0.5$ corresponds to the *maximum* barrier $\max_R F_f(R, h)$. The minimum nucleation barrier turns out to be inversely proportional to the field strength,

$$W = 2W_0\alpha^{3/2}E_0/E, \quad E_0 = \sqrt{W_0/R_0^3\varepsilon} \quad (4.1)$$

corresponding to $h = 2R_0\alpha^{1/2}E_0/E \gg \alpha R_0$ where $W_0 \equiv 16\pi\sigma^3/\mu^2$ is the classical nucleation barrier. This dependence is consistent with our data in Figs. 4.8 and Fig 4-3 .

As suggested by the filament free energy F_f and illustrated in Fig. 4-2, turning the field off makes the filament unstable when its radius is less than $0.5R_0$. Such field outage is naturally achieved by the filament shunting the system; hence, a negative feedback capable of destroying the filament unless it had time to grow its radius above

$0.5R_0$. The required growth is faster when the temperature is higher, which can be facilitated by the liberated Joule heat; hence, stable (unstable) switching for high (low) currents.

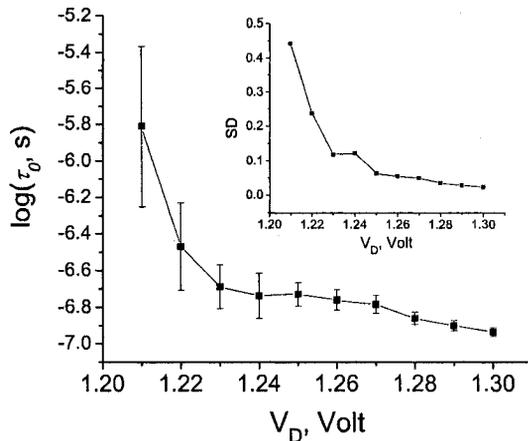


Figure 4-3: Logarithm of switching time as a function of voltage V_D with error bars showing the standard deviation for the same device measured more than 400 times. Shown on the inset is the standard deviation of $\log \tau$.

Finally, a mathematical relationship between the threshold voltage and the delay time (or incubation time) of this cylindrical embryo in the amorphous layer thickness l was developed by V.G.Karpov and Y.A.Kryukov (see Appendix B) [97, 98],

$$V_{th} = \frac{V_{max}}{\ln(\tau/\tau_0)} \quad \text{with} \quad V_{max} = 2l \frac{W_0}{kT} \sqrt{\frac{\alpha^3 W_0}{\epsilon R_0^3}}. \quad (4.2)$$

The characteristic voltage V_{max} (~ 10 V for $l=50$ nm) corresponds to the minimum induction time $\tau = \tau_0$. Assuming nucleation without diffusion [79, 88] suggests the vibrational time $\tau_0 \sim 10^{-13}$ s. Using the latter in combination with the experimental time of, say, $\tau \sim 100$ ns predicts $V_{th} \sim 1.4$ V consistent with the typical data. This

result appears quite unique as relating the observed threshold voltages to the PCM material parameters and thickness. Also developed for experimental verification an equation relating switching delay time, critical nucleation energy, external bias & characteristic voltage,

$$\tau = \tau_0 \exp\left(\frac{W_0 \tilde{V}}{kT V}\right) \quad \text{when } V > \tilde{V} \quad (4.3)$$

predicts that increasing temperature or allowing longer observation time will make switching possible under lower voltages V . Such 'under-threshold' switching will be evidenced in the long lasting high resistance that eventually drops down abruptly, in the manner of standard switching. Furthermore, for low voltages $V \lesssim \tilde{V}$, our consideration predicts a qualitatively different behavior with high resistance state *gradually* decreasing due to onset of spherical crystal nuclei forming a percolation cluster [95].

4.3 Experimental

Experimental verification of the model was performed on Intel devices. These devices were prepared using various state of art recipes (Intel Confidential). Basically it has GST in between the metal top electrodes and the bottom electrode. After lithography and chemical mechanical polishing the patterned GST was exposed to the probes for electrical testing.

The devices were initially programmed to RESET (high resistance, amorphous

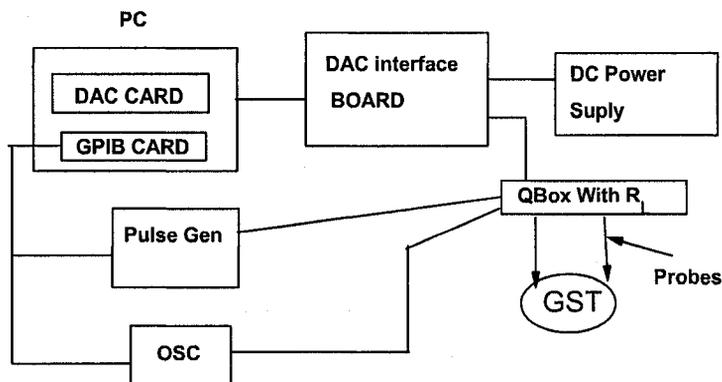


Figure 4-4: Block diagram of the measurement circuit for initial programming. GPIB (General Purpose Interface Bus), DAC (Digital Analog Converter), OSC (Oscilloscope) were used as the basic components in the measurement circuit.

state) with desired current and voltage Figs. 4-4). The basic measurement circuit for these experiments are explained in Fig. 4-4, where the Qbox is a custom made Intel's circuit with a load resistor which basically controls the programmable current through the device. It is connected to the computer through DAC interface card and is powered by a power supply. A pulse generator is connected to one input of the Qbox which basically supplies the electrical pulse to the device under test (DUT) and the output of the Qbox is connected to an Oscilloscope which captures the output signal. There are metal probes which connects the DUT to the Qbox.

Initially, the Intel's device were programmed using this pulse set up in Fig. 4-5. Reset pulse of certain amplitude, width were applied to the devices and correspondingly V_{th} was recorded until the devices were fully reset or thresholds. Then heating was involved to raise the temperatures of the samples to 160c, 167c, 170c and 175c using the setup in Fig. 4-7, knowing the fact that the GST crystallizes above 150c .

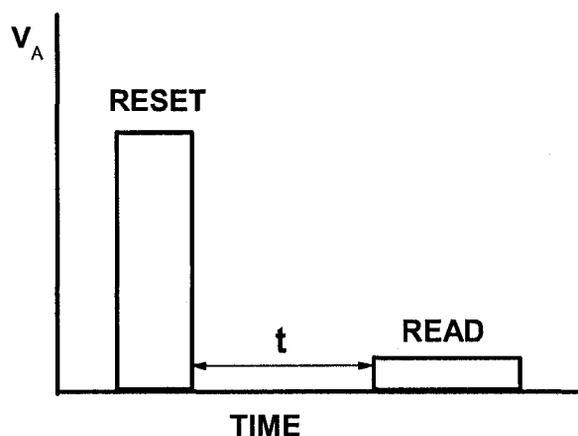


Figure 4-5: Reset pulse to program the device initially

Initially the devices were programmed through a pulse generator and a load resistor with the sample placed on the top of the chuck (which has a heater with temperature measurement set up). After that the temperature of the heater was raised and the sample was heated up. Once it attained the required temperature, the probe tips were lowered. A single reset pulse was applied followed by second read pulse issued from another pulse generator (pulser 2). There is a special way of measuring resistance at high temperature(Fig. 4-6). When the high temperature is attained in the chuck with the sample, then a constant voltage say 0.2, 0.4 and 0.5v was applied for time and current flowing through the device was measured at each interval of that time, and finally the R value was calculated. After the desired temperatures were reached a single RESET pulse was issued followed with a read pulse. Each condition was repeated for at least three devices, and each device was tested not fewer than three times.

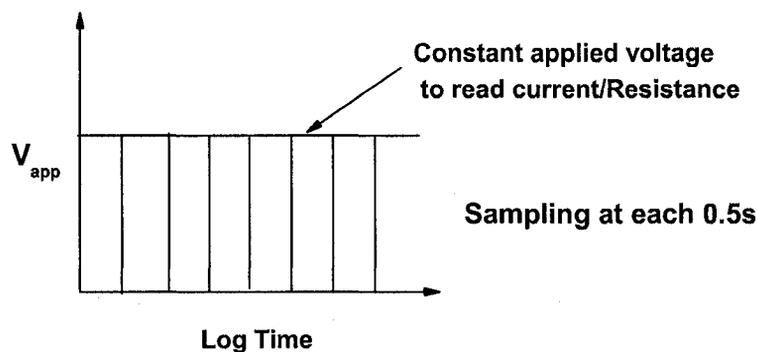


Figure 4-6: Sampling method for measuring R

We observed indeed the phenomenon of resistance abruptly dropping down to crystalline state values after certain times that exponentially decrease with bias and temperature (Fig. 4-9). Fig. 4-8 shows the plot of time to crystallize vs. temperature at different read biases. So higher the temperature and read bias, the less time it took to crystallize.

The moderate *increase* in resistances before their major drop (PCM parameter drift) is caused by long lasting relaxations in the amorphous phase. A thermal analysis was carried out using a 3D model of GST and top electrode to estimate the temperature increase due to applied bias (see section 4.4: Thermal Analysis): it was found rather insignificant (less than 3 K) and unable to explain the observed drop in resistances.

The curves in Fig. 4-9 shift with bias as a whole; the abrupt changes in resistances look similar indeed to the ones known with the standard switching process. characterized by the $V_{th} \approx 1.3$ V and $\tau \gtrsim 100$ ns for our devices). Our data are consistent with Eq. 4.2: the resistance drop time exponentially decreases with temperature and

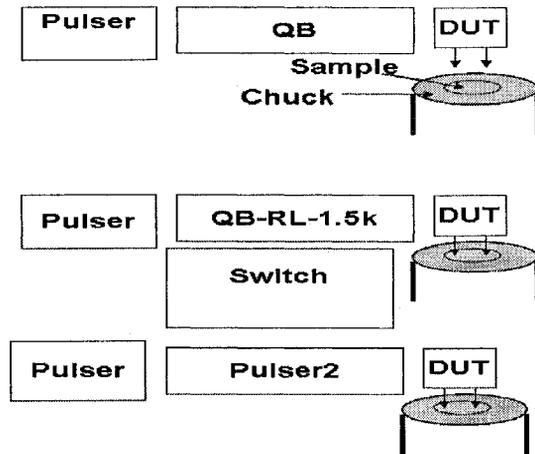


Figure 4-7: Experimental set ups after the devices were initially programmed

voltage. To verify these trends more quantitatively, Fig. 4-10 presents the dependence of resistance drop time vs. $1/V$ and $1/kT$: a good agreement was observed including the above estimate for \tilde{V} . However, the intersect $V^{-1} = 0$ in Fig. 4-10 (a) gives $\tau_0 \sim 1$ s, much higher than the assumed $\tau_0 \sim 10^{-13}$ s. A similar inconsistency of the preexponential obtained by extrapolating data to the region of short times is typical of many glasses and remains poorly understood [96].

We have verified the prediction of short-lived low resistive state by applying voltage pulses of different widths. As expected, a stable resistance change takes place starting with certain pulse width [Fig. 4-11, (a)] showing, in comparison with Fig. 4-9, that time under bias is not less important than time under elevated temperature. Our observation is consistent with the fact that embryos created in strong AFM fields disappear with field removal unless their sizes exceed certain value [94], and with the observations that turning the voltage off shortly after switching takes the system back

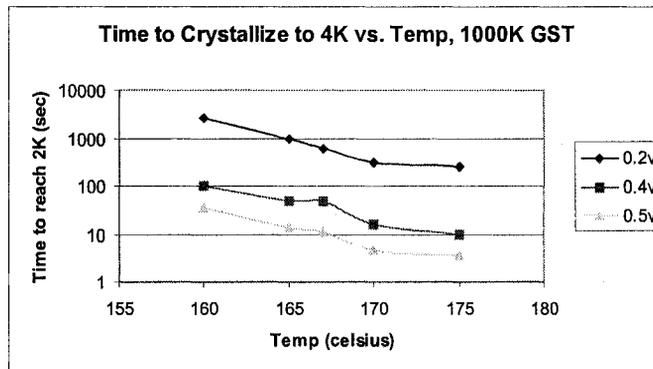


Figure 4-8: Time to crystallize vs. Temperature

to resistive state [60]. Fig. 4-11 (b) shows a related experiment where shorter delay times correspond to lower V_{th} in agreement with Eq. (B.9).

As seen from Fig. 4-9, the lowest voltage (0.2 V) causes a more gradual resistance decrease resembling the behavior in devices observed under zero bias and attributed to percolation cluster of spherical nuclei [95]. The voltage 0.2 V in the experiments was close to \tilde{V} , consistent with its estimate in the above. Another set of experiment was carried out at Intel to verify that the field induced crystallization can take place even at room temperature. The experimental design is explained in Figure. 4-12, where a Reset pulse of certain amplitude and pulse width were issued to initially program the device. After the devices were programmed, they were left to drift for a day, followed by a read pulse of amplitude comparable to the threshold voltage of the device, (pulse width .01s to 120s) but below V_{th} were applied to read the devices. The devices thresholds at room temperature (Fig. 4.13) showing that crystalline state can

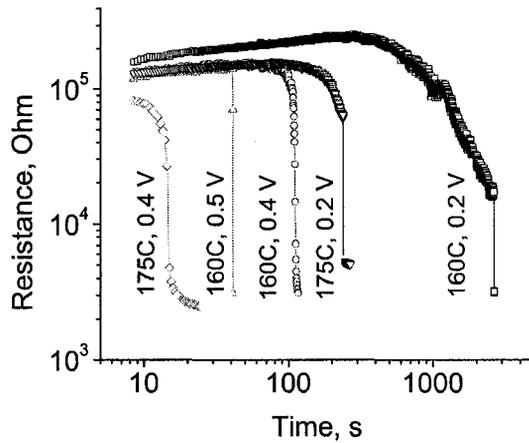


Figure 4-9: High temperature switching reflected in the resistance drop takes place after the delay times increasing with lowering the voltage V_D and the temperature T (shown to the left of the corresponding curve) .

be achieved without temperature effect and under lower read voltage (i.e applied field to induce crystallization) below V_{th} . In Fig. 4.13 we see that applying an input pulse of 1.0v and 1.07v, to a device whose $V_{th} = 1.37v$ generates switching in about 29s and 5s (certain drop in output of the device from 1.4v to 1.0v).

4.4 Thermal Analysis

The goal of this analysis was to rule out a possibility of switching due to the heating (rather than the field induced) effect. The basic structure of those PCM devices has GST as the top electrode and a metal as bottom electrode (see figure 4-14). Though, the current flows through this electrode, which in turn heats the GST but, it is proved by thermal analysis based on a 3D model of GST as top electrode and metal as bottom electrode, that the temperature rise due to this current flow was

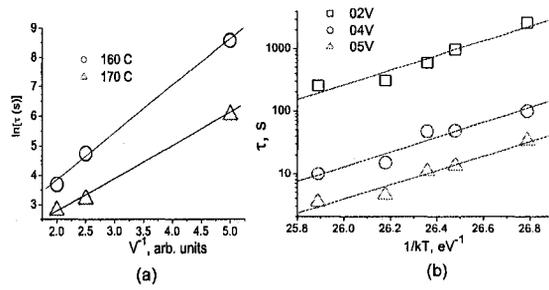


Figure 4-10: Voltage dependence (a) and temperature dependence (b) of switching delay time. Linear fits: Eq. (B.10).

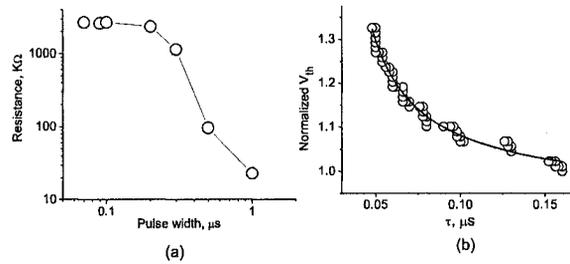


Figure 4-11: (a) Stable resistance change as a function of the potential pulse width in the case of pulse triggered switching. The gradual decay of R corresponds to partial switching. (b) Normalized threshold voltage vs. the corresponding average switching time. The curve is fit by Eq. (B.9).

maximum 1 degree change in Kelvin at the highest bias/read voltage of 0.5v, which is indeed too low to cause a structural change in GST.

The exact solution for this classical thermal model problem is based on 3 boundary conditions: 1. Temperature at the start of bottom electrode, $x=0$ and at the other end, $x=L$ is at 300 K. 2. At the interface ($\sim 1000\text{\AA}$ from the bottom), the total flux entering is equal to the total flux leaving the interface. 3. At the interface, temperature of GST and the bottom electrode is same. The total length of the device $L \sim 1500\text{\AA}$, being the combined length of bottom electrode and GST as top

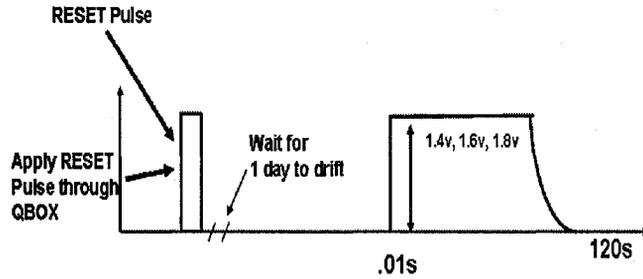


Figure 4-12: Experimental design for under threshold event

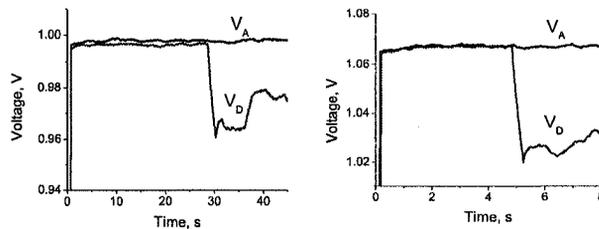


Fig. 2

Figure 4-13: Long-time room temperature switching triggered by voltages well below the threshold voltage, which for the illustrated device was $V_{th} = 1.37$ V with the standard switching delay time of ~ 10 ns. Switching events took place at $V_D = 1.0$ V (left) and $V_D = 1.07$ V (right), corresponding to respectively $\tau = 29$ s and $\tau = 5$ s.

electrode. Also, it was assumed that the GST in the top electrode of the model is in the amorphous state with $R \sim 100$ k Ω .

Solving the standard analytical expression of heat transport equation for this thermal model based on the boundary conditions, we arrive at the conclusion that temperature change at the interface due to the maximum read voltage 0.5 v is close to 1 Kelvin (Fig. 4-15) . This change in temperature due to current flow through the device is low enough to melt the amorphous top electrode GST to a crystalline GST.

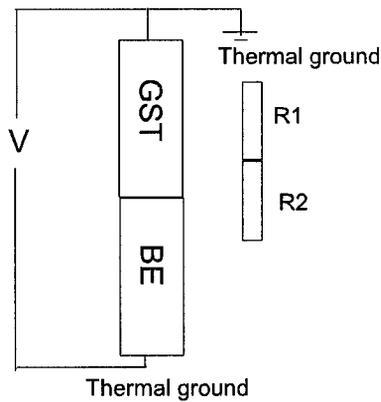


Figure 4-14: 3D model of GST as top electrode and a metal as bottom electrode, assumed as a series network of two resistances with thermal conductivity, $K = 0$ outside the boundary and are thermally grounded at the ends

4.5 Conclusions

In conclusion, we have observed a new phenomenon of *underthreshold* switching below the standard threshold voltages and over the times and temperatures significantly different from those typically reported. This observation is clearly challenging the existing understanding of switching phenomena and calls upon new theoretical insights. One such insight qualitatively developed in the present work is the field induced nucleation mechanism of switching. Its formal development by V. G. Karpov and Y. A. Kryukov (see Appendix B) provided more quantitative predictions consistent with the facts. From a very general point of view, the nucleation switching mechanisms turns out to be a new type of nucleation described in a multidimensional space of parameters (cylinder nucleus length and diameter). More experimental and theoretical work is called upon to further develop this field. Some of the related most recent experimental results remain beyond this thesis, waiting for the Intel confiden-

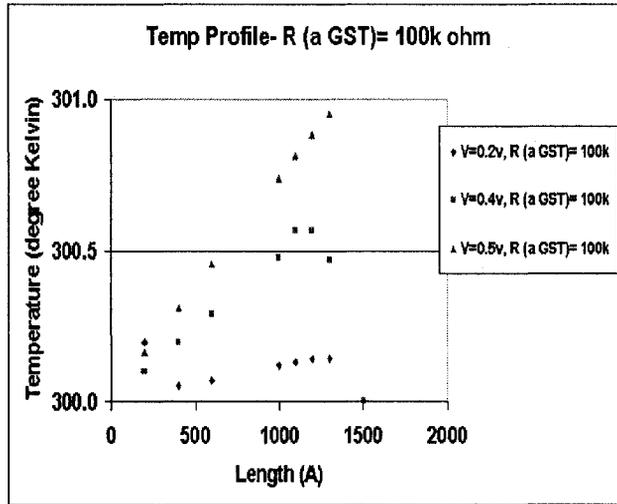


Figure 4-15: Temperature gradient of amorphous GST (top electrode) and a metal (bottom electrode) at different read biases ranging from 0.2v to 0.5v

tial clearance.

Chapter 5

Conclusions

This work describes the electro structural transformations in chalcogenide based thin film devices used in photovoltaics and phase change memory.

CdS layer in CdTe/CdS solar cells was studied extensively and it was found that (1) it acts as piezo/ pyro active system with CdS grains in thin polycrystalline films possessing electric polarization and acting as electric dipoles with preferential axes along the c axis of the crystal; this polarization can be beneficial to PV parameters and technologically forgiving. (2) Three experimental setups with squeezing, bending and flexing deformations showed strong piezo effect in CdS. (3) Xray diffraction show predominantly hexagonal CdS grain orientation along c -axis (002) in a *working device*. (4) The present work suggests new venues in PV technology, such as film deposition and treatments under external bias or light, and purposely created mechanical stresses in CdS through the deposition parameters, tangent layer morphology, or doping. (5) New experimental verifications are suggested, including C-V measurements and ultrasound induced variations in V_{oc} . In general, the above results call upon further work

on piezo- (pyro-) PV coupling including both the experimental work and theoretical modeling.

Electro structural transformations are also studied in chalcogenide based phase change memory devices. The phenomena of PCM switching and temporal drift of parameters of PCM have been experimentally studied in detail.

A significant additional experimental data on drift dynamics of PCM parameters were presented in the current work together with the explanations based on the classical double well potential concept. The important findings from these experimental data are:(1) The drift observation range extended to almost nine decades in time.(2) The drift saturates for both V_{th} and R at long enough time, which is $\sim 10^4$ s at $T = 75$ C and is predicted to be $\sim 10^7$ s at room temperature.(3) Some simple analytical expressions for the observed temporal dependencies, including numerical parameters, were presented based on classical double well potential concepts.

Finally, we have observed and explained a new phenomenon: underthreshold switching in chalcogenide glasses of phase change memory. We have shown that (1) switching can occur under voltages significantly lower than the threshold, (2) over times by many orders of magnitude lower than the typical threshold time, and (3) the switching time follows Arrhenius behavior as a function of both temperature and voltage. Our findings clearly favor a nucleation mechanism of switching that was unduly ignored in the community for almost 50 years.

Appendix A

Piezo & Pyro Photovoltaic Coupling

A.1 Device operations and Model

This Appendix describes the results of the numerical modelling of the device performance in the presence of a polarized CdS layer following the work by M. L. C. Cooray and V. G. Karpov [49,59]. The work presented here used the AMPS software developed at the Pennsylvania State University by S. Fonash et al. Its development was supported by the Electric Power Research Institute. The term AMPS abbreviates "Analysis of Microelectronics and Photonic Structures" and represents a computer code which allows the analysis of a broad variety of device structures under illumination or voltage bias or both. A detailed description of the solution techniques can be found in the AMPS manual [46]. The modelling is significantly based on the AMPS generated models [46] of the structure composed of the following layers: (1) TCO

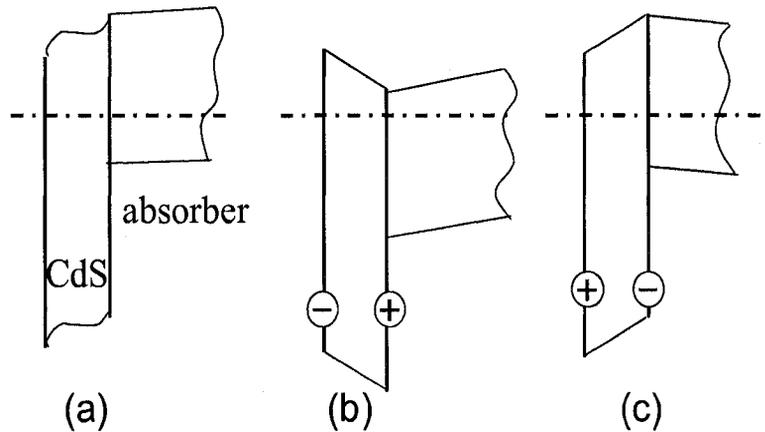


Figure A-1: Conceivable band diagrams of CdS based PV. (a) p-n structure with n-type CdS and p-type absorber. (b) A 'gull wing' potential shape structure; (+) and (-) mark the polarization charges. (c) The 'hunch' model where electric field in CdS region allows for carrier collection. Dot-dashed lines show the Fermi level. For simplicity, the conduction band offset between the CdS and absorber is set to zero.

(transparent conductive oxide) playing the role of a metal contact; (2) slightly n-type CdS window layer (thickness 100 nm, donor concentration $2 \cdot 10^{16} \text{ cm}^{-3}$); (3) two artificial very thin CdS layers (10 nm) tangent to both sides of the layer (2) strongly doped with donors and acceptors and aimed at mimicking the electric polarization charges; [47] (4) p-CdTe absorber with acceptor concentration of 10^{14} cm^{-3} . The three possible device band diagrams are shown in Fig A1. It was verified that adding the recombination centers suggested in Ref. [48] has a rather insignificant effect (of several relative percent) on the simulated parameters of models (b) and (c), unlike their known strong effect on the 'standard' p-n junction structure (a), meaning that the model (b) is extremely forgiving from the point of view of material quality.

Fig. A-1 (a) represents the 'main-stream' model of p-n type device with rather insignificant electric field in the CdS region that does not contain the strongly doped

layers. This model (whose parameters here are not fine-tuned) is aimed at representing a reference point convenient for comparison with the dipole layer models.

Related to the potential distribution in Fig. 2-8 is the 'gull-wing' model of Fig. A-1, (b) that describes a number of experimental facts [49], such as the lack of carrier collection from CdS [8, 50] due to the field reversal according to this model. The corresponding barrier in Fig. A-1, (b) is consistent with the CdS depletion and was independently suggested earlier based on a different argument. [51] Another feature of that model is that, under illumination, the electrons accumulated in the "gull wing" region will generate the electric field suppressing the barrier. Hence, the electric current increase leading to the dark and light JV crossing, qualitatively consistent with the CdS photoconductivity. [53] On the other hand, the CdS barrier will limit forward current causing $J(V)$ flattening (rollover) in the forward bias region. Characteristic of this model is the CdS polarization enhancing the electric field in the absorber layer (as explained in the above Sec. 2.2.3) thus improving the carrier collection and V_{oc} . One consequence of such an electric field amplification is that the absorber layer inverts its conduction type close to the singularity; for example, the p-type CdTe becomes n-type in the proximity of the CdS layer. The hypothesis of CdTe inverting its conduction type has been put forward earlier on different grounds. [51, 52]

The case of the opposite CdS polarity and negative fields in Fig. A-1 (c) also has a strong effect on the electric field in the absorber. The underlying physics is that it creates the potential barrier for the electrons thus blocking the current from the absorber. On the other hand, this polarization allows for the collection of carriers generated in the CdS region (by high energy photons with wavelengths $\lambda < 520$ nm).

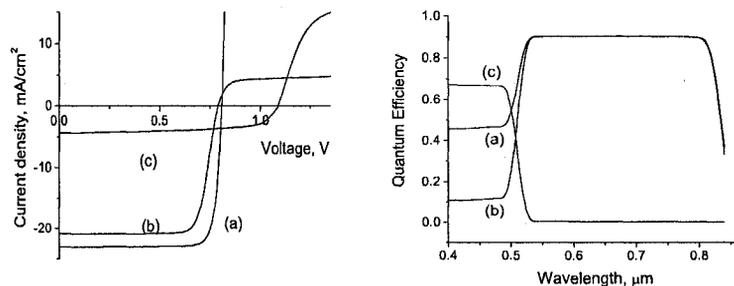


Figure A-2: AMPS [46] generated light $J-V$ characteristics and quantum efficiencies (QE) for three different device models: the standard p-n junction (a), gull wing potential (b), and the opposing field model(c).

The results of AMPS modelling of current-voltage characteristics and quantum efficiencies (Fig. A-2) show a qualitative similarity between the standard p-n and gull wing models. An important difference is that the p-n model here allows for the carrier collection from CdS. To suppress the latter feature the existing more refined p-n junction models assume a very high concentration of recombination centers in CdS region in order to suppress the corresponding carrier collection never observed experimentally. [48, 50] We note that the curve (c) in Fig. A-2 represents the current generated in the CdS region and does not show contribution from the CdTe layer. The quantum efficiency (QE) curves further confirm the above interpretation: lack of carrier collection from CdS in the gull-wing model, and lack of the carrier collection from the CdTe region in the 'hunch' model of Fig. A-1 (c).

The results of the above described modeling for the major PV parameters are summarized in Fig. 2-22 for a wide range of the CdS electric field strengths; here the positive and the negative field regions correspond respectively to the models (b) and

(c) of Fig. A-1.

From the technological perspective, the range of positive fields ('gull-wing' region) in Fig. 2-22 is more forgiving, since the PV parameters there are relatively independent of the CdS field strength. Moreover, the device efficiency in that region is likely to be better than the AMPS predicted values due to the current leakage through the CdS barrier, which is not accounted for by AMPS modelling.

We conclude that dipole layers have a strong effect on device operations and further broaden the scope of parameters in thin-film PV technologies. A region of not very large positive CdS fields appears most attractive technologically. This field region likely corresponds to the case of equilibrium polarization discussed in Sec. 2.2.3. However, because the PV parameters are not very sensitive to the polarization strength in the 'gull-wing' shaped potential region, the performance difference between the frozen-in and the equilibrium polarization cases in Sec. 2.2.3 and 2.2.3 may be relatively insignificant.

Appendix B

Model of field Induced Nucleation in Phase Change Memory

Here we briefly describe the theoretical model [97,98] developed by V. G. Karpov and Y. A. Kryukov for the observed field induced switching phenomena.

The electric field effect on nucleation is due to a 'metal' (more polarizable phase) nucleus induced increase in the local field strength E and decrease in the electrostatic energy [84,85]

$$E = E_0/n, \quad W_E = -\Omega E_0^2 \varepsilon / (8\pi n) \quad (\text{B.1})$$

where ε is the dielectric permittivity and E_0 is the uniform field far from the particle. The depolarization factor $n = 1/3$ for a spherical particle, while for a long cylinder of length h and radius R it takes the form

$$n = (1/\xi)^2 [\ln(2\xi) - 1], \quad \xi \equiv h/R \gg 1. \quad (\text{B.2})$$

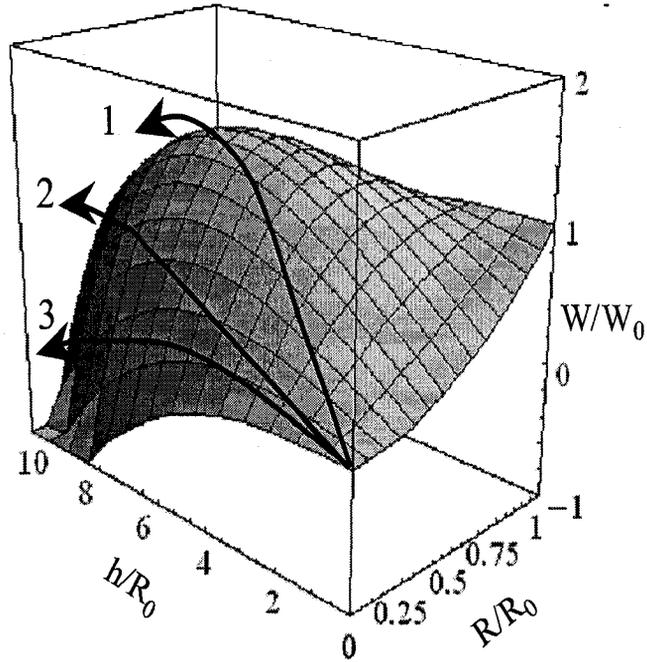


Figure B-1: Free energy of Eq. (B.4) as a function of the cylinder radius R and length h . The arrows illustrate possible phase transformation pathways: 1 passes through the maximum nucleation barrier, 2 follows the transformation path at fixed $\xi = h/R$ corresponding to Eq. (B.5), 3 shows that yet lower nucleation barriers may be possible.

The nucleation switching in high electric field between two flat electrodes starts with a cylinder shaped conductive crystal embryo. Similar to lightning rod, the cylinder concentrates the electric field, which then facilitates nucleation of additional particles at its end, further

increasing its length, the field strength, etc. This instability leads to a low resistive crystalline filament shunting across the structure. The embryo induction time $\tau = \tau_0 \exp(W/kT)$ is interpreted as the switching delay time (between the voltage application and the switching event). On experimental grounds, it must be short

enough (say, $\tau \lesssim 10^{-7}$ s), thus requiring a rather low nucleation barrier W .

As a baseline, consider nucleation of a spherical particle in electric field E_0 . In its free energy $F(R) = 4\pi R^2\sigma - 4\pi R^3\mu/3 - R^3E_0^2\varepsilon/2$, the first two terms represent interface and bulk contributions [86], and the third one accounts for the electrostatic energy W_E . The nucleation barrier $W = \max[F(R)]$ is given by

$$W = W_0(1 + \zeta/4)^{-2}, \quad \zeta \equiv E_0^2 R_0^3 \varepsilon / W_0 \quad (\text{B.3})$$

where

$$R_0 = 2\sigma/\mu \quad \text{and} \quad W_0 \equiv 16\pi\sigma^3/3\mu^2$$

are respectively the critical nucleation radius and energy. For numerical estimates, we use the typical, $W_0 \approx 2$ eV, $R_0 \approx 3$ nm, [87] $\varepsilon = 16$ and switching field strength of $E_0 \approx 3 \cdot 10^5$ V/cm, which yields $\zeta \approx 0.1$, hence $W \approx W_0$, i. e. field effect on nucleation barrier is relatively small.

Cylinder-like particles aligned to the field will gain more electrostatic energy. For a long cylinder, the free energy is given by

$$F_c = 2\pi R^2\sigma + 2\pi R h \sigma - \pi R^2 h \mu - h^3 E_0^2 \varepsilon / 8. \quad (\text{B.4})$$

where we have neglected the logarithmic factor in Eq. (B.2). Its stationary point $\partial F/\partial h = \partial F/\partial R = 0$ is a maximum at $R = R_0/2$ and $h/R = 2/\sqrt{\zeta}$. It is important that the parameters space here is two-dimensional (R and h) and the system can find nucleation pathways through lower barriers than the maximum as illustrated in

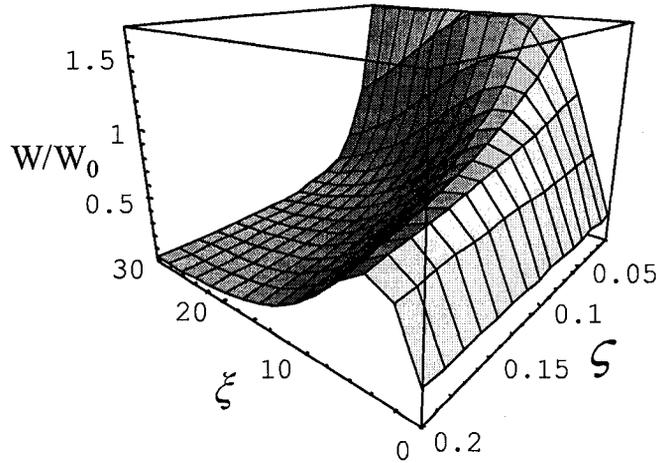


Figure B-2: Nucleation barrier of Eq. (B.5) corresponding to the transformation with fixed $\xi = h/R$ as a function of cylinder proportion ξ and field strength parameter ζ .

Fig. B-1. This flexibility makes cylinder nucleation different from that of spherical particles where one-dimensional parameter space (R) makes the maximum energy point unavoidable. We show next that in a strong electric field, the cylinder nucleation barrier can be considerably lower than W_0 .

Following [79] consider first nucleation along the path of fixed $h/R = \xi$ [cf. Eq. (B.2)]. Substituting $h = R\xi$ in Eq. (B.4) and optimizing it with respect to R yields

$$W = W_0(2/9)(\xi + 1)(1 + \zeta\xi^2/12)^{-2}. \quad (\text{B.5})$$

As illustrated in Fig. B-2, the barrier W for nucleation of a long ($\xi \gg 1$) cylinder in a strong field can, in principle, be much lower than W_0 . However the realistic switching fields with $\zeta \lesssim 0.1$ are not strong enough to fully utilize that effect. In addition, there exist other nucleation pathways with lower barriers as shown next.

As seen from Fig. B-1, low barrier nucleation pathways generally correspond to the region of small R . Eq. (B.4) shows that formally the pathways of infinitesimally small R traverse through the correspondingly low barriers. In reality, several factors set lower bound to the radii of nucleating cylinders. These are, for example, the failure of the interfacial energy (σ) concept for R comparable to interatomic distances, and mechanical stresses between the two phases capable of rupturing too thin cylinders. Also, the low resistivity of the crystalline state may not translate into the cylinder low resistance if its radius is small enough. These and other size limitations will be accounted for by introducing a minimum radius, αR_0 , below which the conductive crystalline cylinder does not exist; α remains a dimensionless phenomenological parameter in the range of $0.1 \lesssim \alpha \lesssim 0.5$ ($\alpha = 0.5$ corresponds to the maximum point in Fig. B-1).

Along the lines of classical nucleation theory, a future stable embryo grows continuously in the parameter space (R, h) inevitably crossing (or touching) the minimum radius line $R/R_0 = \alpha$ as illustrated in Fig. B-3. The iso-free-energy contour touching that line will correspond to the minimum barrier W in a plurality of ways leading to a stable embryo. It is determined by the equations

$$\min[R(h, W)] = \alpha R_0 \quad \text{and} \quad F_c(R, h) = W \quad (\text{B.6})$$

with $F_c(R, h)$ from Eq. (B.4). Taking into account $\zeta \ll 1$ and omitting straightforward arithmetic yields

$$W = 2W_0(\alpha^3/\zeta)^{1/2}, \quad (\text{B.7})$$

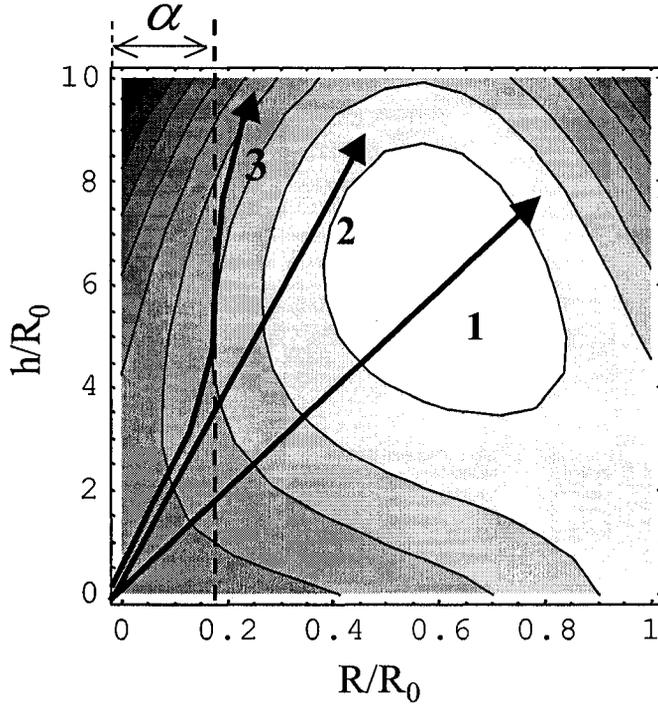


Figure B-3: Contour plot of the energy surface and nucleation pathways from Fig. B-1.

corresponding to the embryo parameters

$$R = \alpha R_0, \quad \text{and} \quad h = 2R_0(\alpha/\zeta)^{1/2} \gg R. \quad (\text{B.8})$$

For a rough guide numerical estimate we use the above $\zeta \approx 0.1$ and arbitrary $\alpha = 0.1$, which gives $W \approx 0.3W_0$. We conclude that the field induced nucleation barrier change can be significant. Our results here are limited to homogeneous nucleation.

Because of $\xi \gg 1$ [cf. Eq. (B.8)] the electric field $E = E_0\xi^2$ at an embryo tip becomes strong enough to trigger secondary nucleation quickly shunting through the rest of amorphous structure. We note, however, that a just formed embryo may be

unstable with respect to field removal. Indeed, Eq. (B.4) shows that, under zero field conditions, a long cylinder remains stable when $R > R_0/2$. Therefore, a just nucleated cylinder of radius $\alpha R_0 < R_0/2$ will decay unless the field is maintained long enough to grow its radius beyond $R_0/2$. Experimentally, this will result in a short-lived low-resistive state lasting until the field is removed.

Another verifiable result of our theory is the threshold voltage switching the system with a given delay time τ . Substituting into Eq.(B.7) ζ from Eq. (B.3) and $W = kT \ln(\tau/\tau_0)$ yields the electric field, which is related to V_{th} through the amorphous layer thickness l ,

$$V_{th} = \frac{V_{max}}{\ln(\tau/\tau_0)} \quad \text{with} \quad V_{max} = 2l \frac{W_0}{kT} \sqrt{\frac{\alpha^3 W_0}{\epsilon R_0^3}}. \quad (\text{B.9})$$

The characteristic voltage V_{max} (~ 10 V for $l=50$ nm) corresponds to the minimum induction time $\tau = \tau_0$. Assuming nucleation without diffusion [79, 88] suggests the vibrational time $\tau_0 \sim 10^{-13}$ s. Using the latter in combination with the experimental time of, say, $\tau \sim 100$ ns predicts $V_{th} \sim 1.4$ V consistent with the typical data. This result appears quite unique as relating the observed threshold voltages to the PCM material parameters.

Another characteristic voltage $\tilde{V} = V_{max} kT/W$ (~ 0.1 V for $l \sim 50$ nm) corresponds to $W = W_0$ in Eq. (B.7). Below \tilde{V} , the switching concept fails, giving up to nucleation of spherical particles.

Rewriting Eq. (B.7) in the terms of switching delay time,

$$\tau = \tau_0 \exp\left(\frac{W_0 \tilde{V}}{kT V}\right) \quad \text{when } V > \tilde{V} \quad (\text{B.10})$$

predicts that increasing temperature or allowing longer observation time will make switching possible under lower voltages V . Such 'under-threshold' switching will be evidenced in the long lasting high resistance that eventually drops down abruptly, in the manner of standard switching. Furthermore, for low voltages $V \lesssim \tilde{V}$, our consideration predicts a qualitatively different behavior with high resistance state *gradually* decreasing due to onset of spherical crystal nuclei forming a percolation cluster [95].

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