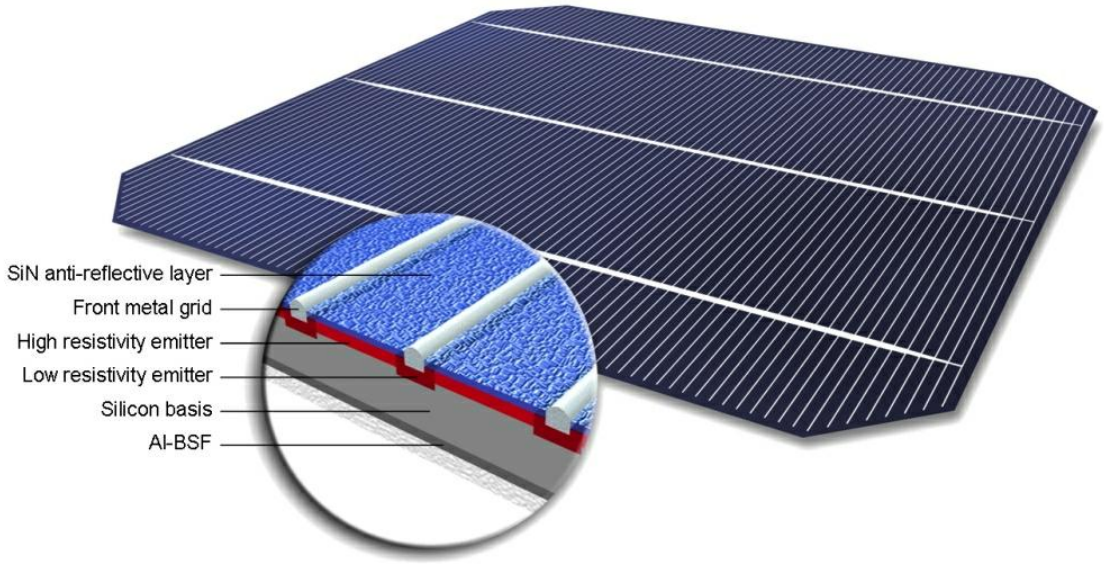
Crystalline Silicon PV Technology



March 25, 2014

Principles and Varieties of Solar Energy (PHYS 4400)
The University of Toledo, Department of Physics and Astronomy

Missed Classes -- recovery schedule

- March 27, start at 11:50 am
- April 1st, class from 11:50 am – 2:20 pm
- April 10, start at 11:50 am

Revisiting the J-V dependence of a solar cell

- More detailed look at J(V) behavior;
- Temperature dependence of V_{OC};
- Intensity-dependence of V_{OC};

- then… C-Si PV

The simple J-V curve (ideal diode equation)

$$I = I_0\left(e^{\frac{qV}{kT}} - 1\right)$$

Add light:

$$I = I_0\left[\exp\left(\frac{qV}{kT}\right) - 1\right] - I_L$$

In terms of J (and reverse sign to bring the J-V curve's power-generation into the 4th quadrant):

$$J = J_{SC} - J_0\left[\exp\left(\frac{qV}{kT}\right) - 1\right]$$

Now consider the case where the contacts are isolated (open circuit)

The current density J must be = 0 mA, and we can solve as follows:

$$J = 0 \Rightarrow J_{SC} = J_0\left[\exp\left(\frac{qV_{OC}}{kT}\right) - 1\right]$$

Rearrange to get:

$$V_{OC} = \frac{kT}{q}\left(\ln\left(\frac{J_{SC}}{J_0}\right) + 1\right)$$

How does J_{SC} depend upon incident light intensity?
How does V_{OC} depend on incident light intensity?

Look at temperature dependence of J_0

The current density J must be = 0 mA, and we can solve as follows:

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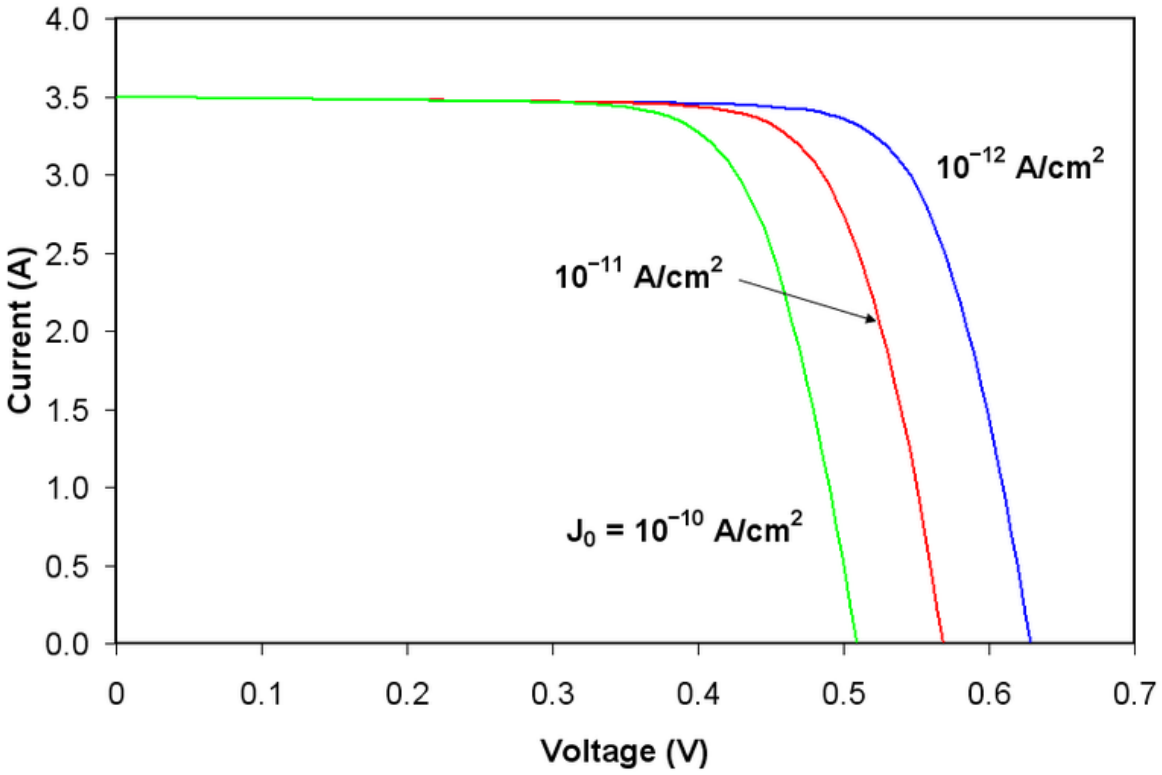
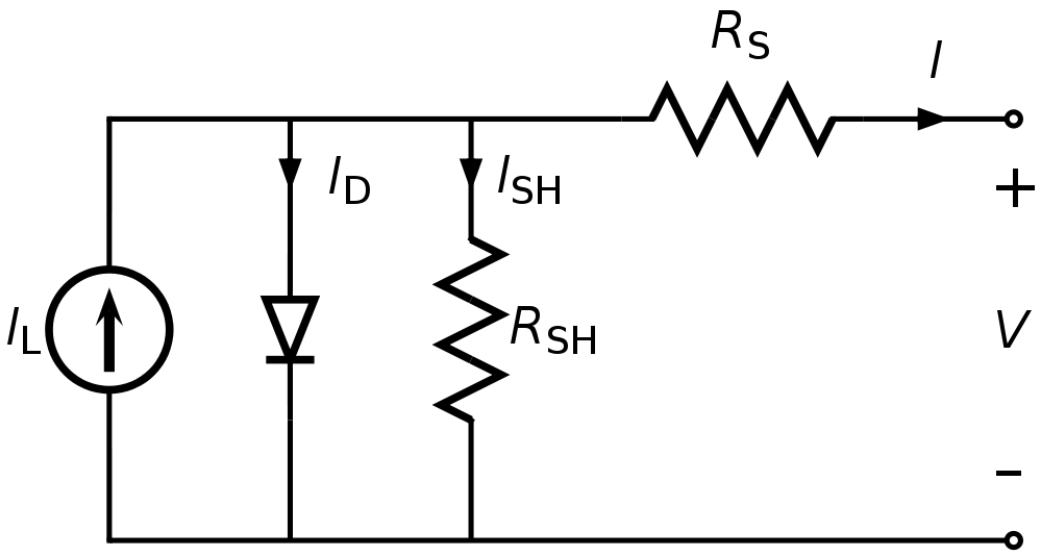


Equivalent Circuit of a solar cell



$$J = J_L - J_D - J_{SH}$$

$$V_j = V + IR_S$$

http://en.wikipedia.org/wiki/Theory_of_solar_cells

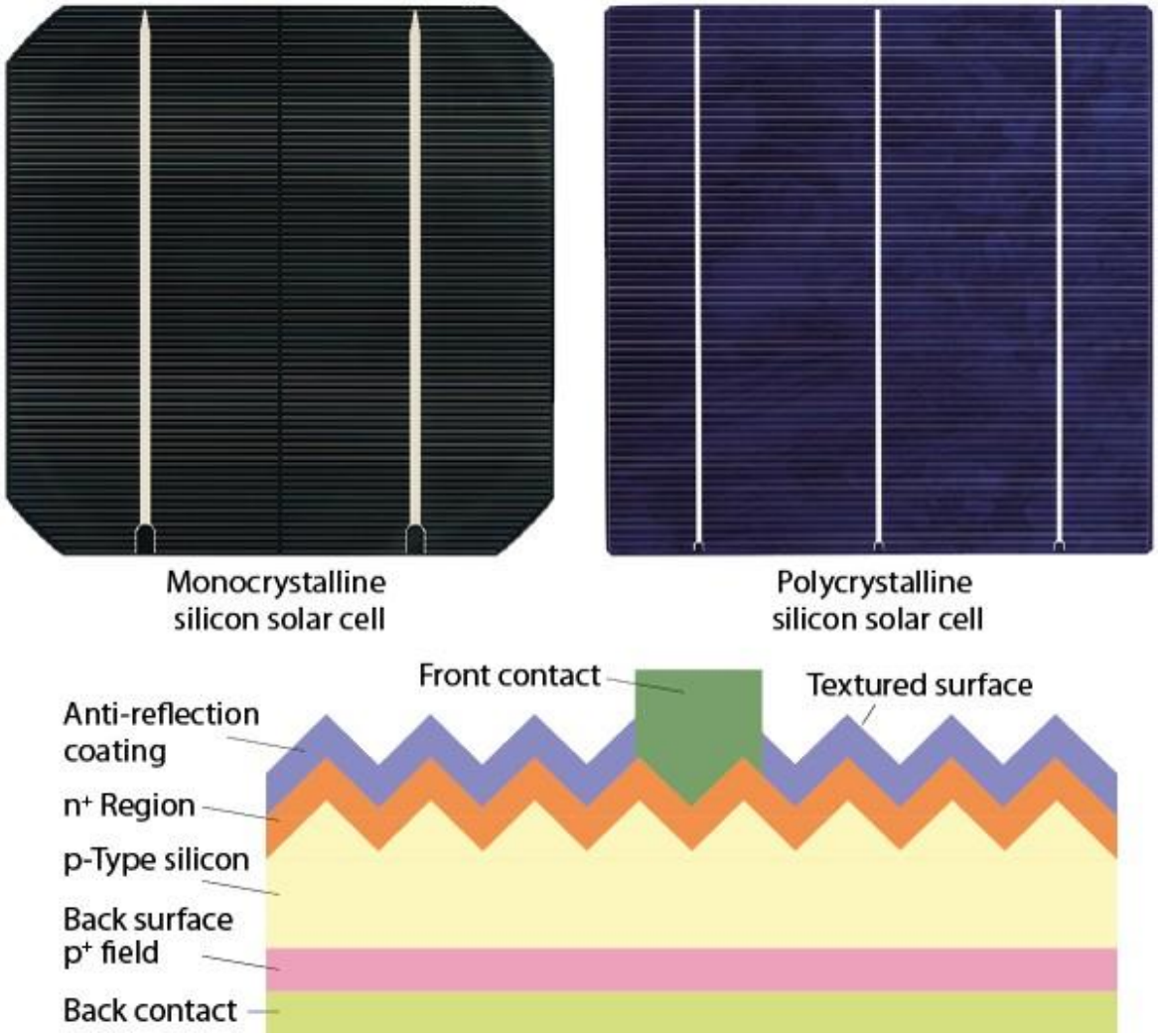
Crystalline/Polycrystalline Silicon PV Technology (some facts)

- Crystalline silicon PV cells are used in the largest quantity of all types of panels on the market, representing ~85% of the world total PV cell production in 2009.
- The highest energy conversion efficiency reported so far for a research-scale crystalline silicon PV cell is 25%.
- Standard industrial scale cells are limited to (polycrystalline Si) ~16% with the exception of certain high-efficiency cells based on monocrystalline Si capable of efficiencies > 20%.
- High-efficiency research PV cells have advantages in performance but may be unsuitable for low-cost production due to their complex structures and the lengthy manufacturing processes required for fabrication.
- World annual production of PV cells reached more than 7.9 GWp in 2008, 10.6 GWp in 2009, 18.6 GWp in 2010, 28 GWp in 2011, and 30 GWp in 2012.
- Average annual growth rate in PV cell production/installation over the last decade has been ~40% (CAGR). Cumulative installed capacity is ~ 101 GW.
- Electrical power generated by all PV systems around the world is ~0.1% of the total world electricity generation – so the penetration of PV remains low.

Aside: what is Wp?

The use of units Wp, which stands for Watt-peak, is commonplace in reference to the power generating capacity of a PV system. Watt-peak refers to the power generated by a PV module or system under standard illumination conditions of 1000 W/m^2. Actual illumination (insolation) levels vary widely, of course, depending on latitude, time of day, and weather conditions.

Although the "cost per Watt" or "cost per Watt-peak" is a common assignment of cost for a module or system, one must determine the predicted and/or actual energy generated by a system to properly assess the economics of a specific system.



Typical mono- and polycrystalline silicon solar cells (upper), and simplified cross-section of a commercial monocrystalline silicon solar cell (lower) (© 2010 Sharp).

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Production of "Standard" Silicon PV Cells

- Standard cells are produced using monocrystalline and polycrystalline boron-doped (p-type) silicon substrates. Cells are now commonly 156 mm (6 inches) square, respectively.

- Monocrystalline solar cells are typically produced from (single-crystal) pseudo-square silicon wafer substrates cut from column ingots grown by the Czochralski (CZ) process.

- Polycrystalline cells, on the other hand, are made from square silicon substrates cut from polycrystalline ingots grown in quartz crucibles. The front surface of the cell is covered with micrometer-sized pyramid structures (textured surface) to reduce reflection loss of incident light.

- An anti-reflection coating (ARC) of silicon nitride (SiN_x) or titanium oxide (TiO_x) is overlayed on the textured silicon surface to further reduce reflection loss.

- A highly phosphorous doped n+ region is produced on the front surface of boron-doped p-type substrates to form p–n junctions.

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The value chain for crystalline silicon solar cells and modules is longer than that for thin-film solar cells:

- There are generally three industries related to crystalline silicon solar cell and module production:

1. metallurgical and chemical plants for raw material silicon production;
2. monocrystalline and polycrystalline ingot fabrication and wafer fabrication by multi-wire saw;
3. solar cell and module production.

- The cost of PV production is divided roughly in half between solar cell module production and balance-of-system fabrication, which includes the inverter, cables and installation.

- The fabrication cost for solar cell modules includes the cost of the silicon substrate (50%), cell processing (20%) and module processing (30%).

- The cost share is therefore strongly affected by the market price for poly-silicon feedstock, and reducing the cost of the silicon substrate remains a critical issue for the PV industry.

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Production of metallurgical grade Si

Silicon is commercially prepared by the reaction of high-purity silica with wood, charcoal, and coal, in an electric arc furnace using carbon electrodes. At temperatures over 1,900 °C (3,450 °F), the carbon reduces the silica to silicon according to the chemical equations:

$$SiO_2 + C \rightarrow Si + CO_2$$
$$SiO_2 + 2\,C \rightarrow Si + 2\,CO$$

Liquid silicon collects in the bottom of the furnace, and is then drained and cooled. The silicon produced via this process is called *metallurgical grade silicon* and is at least 98% pure. Using this method, silicon carbide (SiC) may form. However, provided the concentration of SiO_2 is kept high, the silicon carbide can be eliminated:

$$2\,SiC + SiO_2 \rightarrow 3\,Si + 2\,CO$$

In September 2008, metallurgical grade silicon cost about USD 1.45 per pound ($3.20/kg),[9] up from $0.77 per pound ($1.70/kg) in 2005.[10]

Pure silicon (>99.9%) can be extracted directly from solid silica or other silicon compounds by molten salt electrolysis.[11][12][13][14] This method, known from 1854[15] (see also FFC Cambridge Process) has the potential to directly produce solar grade silicon without any CO_2 emission and at much lower energy consumption.

From Wikipedia

Purification by Physical Methods

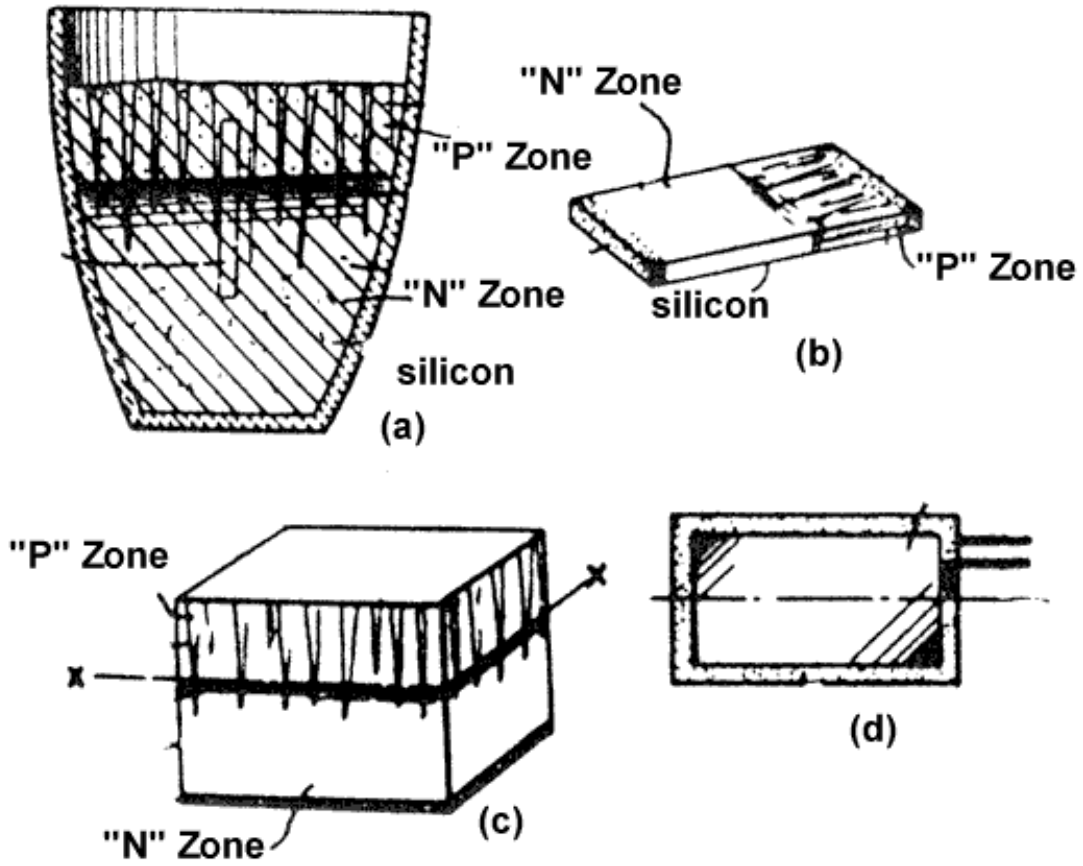
Early silicon purification techniques were based on the fact that if silicon is melted and re-solidified, the last parts of the mass to solidify contain most of the impurities. The earliest method of silicon purification, first described in 1919 and used on a limited basis to make radar components during World War II, involved crushing metallurgical grade silicon and then partially dissolving the silicon powder in an acid. When crushed, the silicon cracked so that the weaker impurity-rich regions were on the outside of the resulting grains of silicon. As a result, the impurity-rich silicon was the first to be dissolved when treated with acid, leaving behind a more pure product.

In zone melting, also called zone refining, the first silicon purification method to be widely used industrially, rods of metallurgical grade silicon are heated to melt at one end. Then, the heater is slowly moved down the length of the rod, keeping a small length of the rod molten as the silicon cools and re-solidifies behind it. Since most impurities tend to remain in the molten region rather than re-solidify, when the process is complete, most of the impurities in the rod will have been moved into the end that was the last to be melted. This end is then cut off and discarded, and the process repeated if a still higher purity is desired.

400 kgs

From Wikipedia

In studies of recrystallized melts of pure silicon prepared for this purpose, Ohl [2] discovered the presence of a well-defined barrier in ingots grown from commercially available, high-purity silicon.



(a) Cast ingot showing natural junction formed by impurity segregation during melting; (b) photovoltaic device cut perpendicular to junction; (c) device cut parallel to junction; (d) top surface of device cut parallel to junction.

From Wikipedia

Purification by Gas Phase Chemical Methods

Today, silicon is purified by converting it to a silicon compound that can be more easily purified by distillation than in its original state, and then converting that silicon compound back into pure silicon. Trichlorosilane is the silicon compound most commonly used as the intermediate, although silicon tetrachloride and silane are also used. When these gases are blown over silicon at high temperature, they decompose to high-purity silicon.

At one time, DuPont produced ultra-pure silicon by reacting silicon tetrachloride with high-purity zinc vapors at 950 °C, producing silicon:

$$SiCl_4 + 2\ Zn \rightarrow Si + 2\ ZnCl_2$$

However, this technique was plagued with practical problems (such as the zinc chloride byproduct solidifying and clogging lines) and was eventually abandoned in favor of the Siemens process.

In the **Siemens process**, high-purity silicon rods are exposed to trichlorosilane at 1150 °C. The trichlorosilane gas decomposes and deposits additional silicon onto the rods, enlarging them:

$$2\ HSiCl_3 \rightarrow Si + 2\ HCl + SiCl_4$$

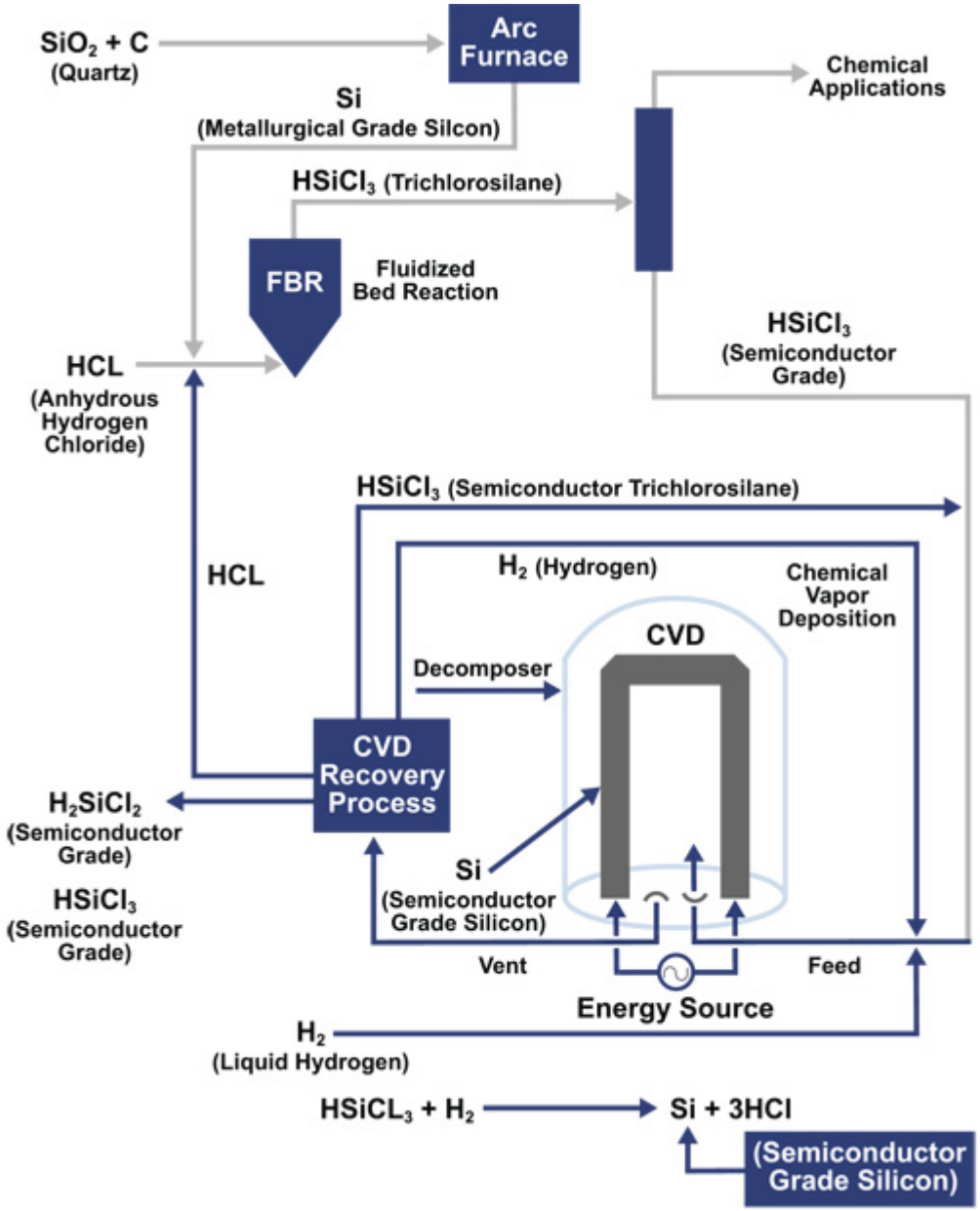
Silicon produced from this and similar processes is called *polycrystalline silicon*. Polycrystalline silicon typically has impurity levels of less than 10^{-9}.

In 2006 REC announced construction of a plant based on fluidized bed technology using silane:[17]

$$3\ SiCl_4 + Si + 2\ H_2 \rightarrow 4\ HSiCl_3$$
$$4\ HSiCl_3 \rightarrow 3\ SiCl_4 + SiH_4$$
$$SiH_4 \rightarrow Si + 2\ H_2$$

From Wikipedia

From quartz rock to hyper-pure poly Si (99.999999999%)



Hemlock Semiconductor Group (HSC) manufactures high-purity poly Si feedstock for the manufacture of solar and semiconductor products. HSC's manufacturing uses trichlorosilane, which is converted to polysilicon in a chemical vapor deposition (CVD) reactor employing a U-rod. All chemicals are captured and recycled.

Impurities are 1 part in 10^{11}, "intrinsic" (i.e. impurity) dopant concentration of ~10^{12} cc^{-1}, or 1 ppt (i.e. 1 part per trillion)

http://www.hscpoly.com/content/hsc_prod/manufacturing_overview.aspx

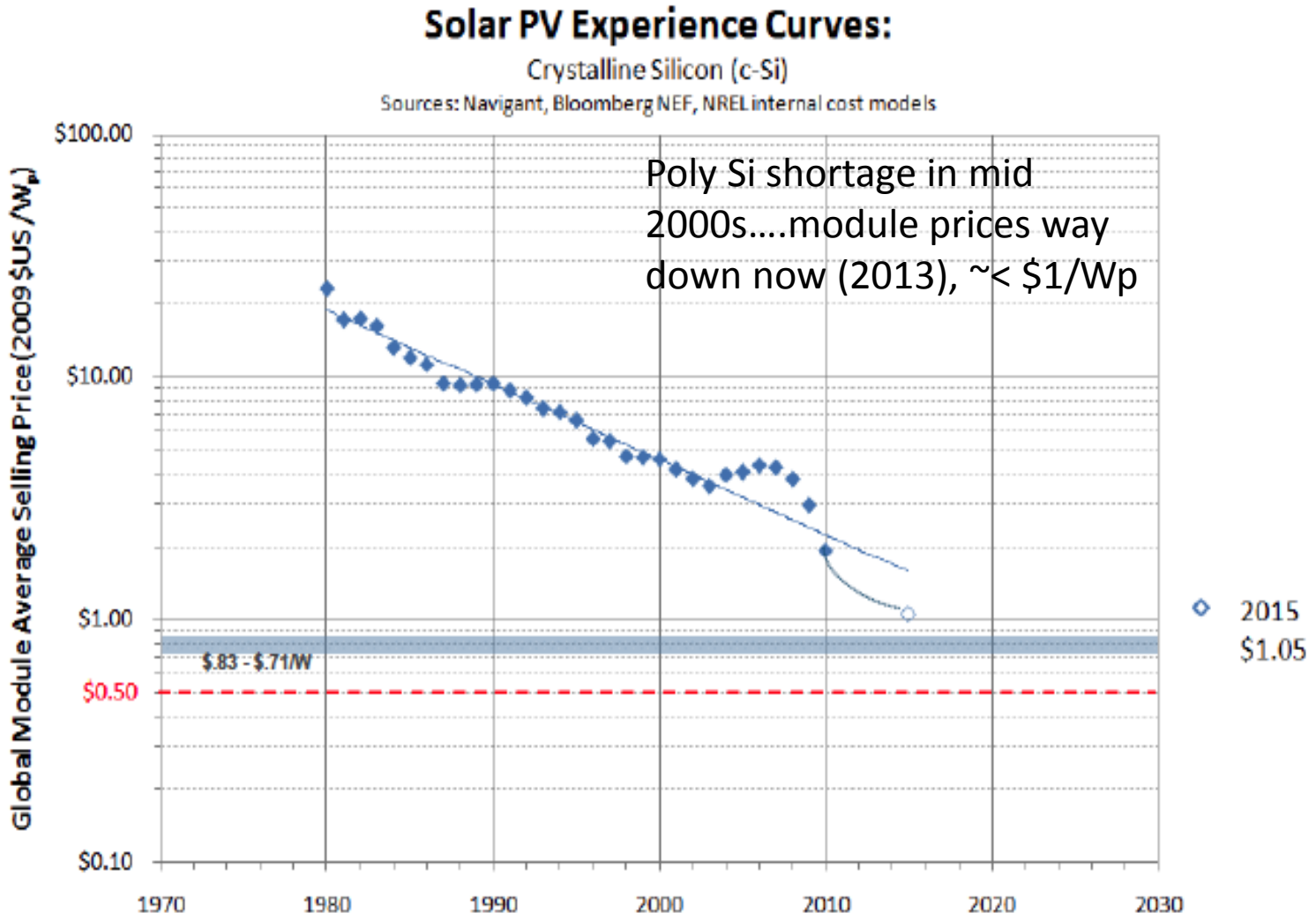
Hemlock Semiconductor Group

- Owned by Dow Corning Corporation (63.25%), Shin-Etsu Handotai (24.5%), and Mitsubishi Materials Corporation (12.25%)
- Began operation in 1961 in Hemlock, Michigan
- Leading world supplier of high purity poly-crystalline silicon to the semiconductor and solar industries
- Currently completing several major expansions in Michigan and Tennessee
- 36,000 metric ton capacity by 2010

http://www.hscpoly.com/content/hsc_home/default.aspx?bhcp=1

Solar PV Cost Reduction Progress, Potential of Known Technology Pathways

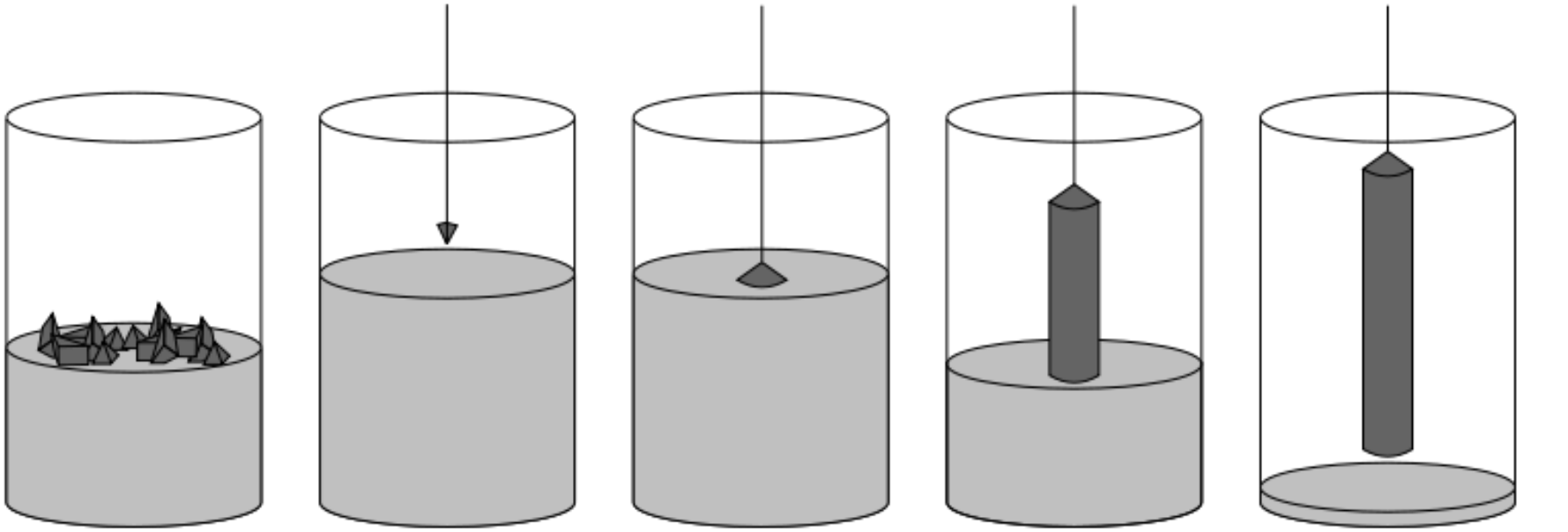
U.S. DEPARTMENT OF ENERGY | Energy Efficiency & Renewable Energy



US net exporter in PV in 2010 (+1.9 B$); $2.5 billion was polysilicon.

http://www.greentechmedia.com/articles/read/stat-of-the-week-positive-us-solar-trade-balance/

From Raw Silica (SiO_2) to Final Cell



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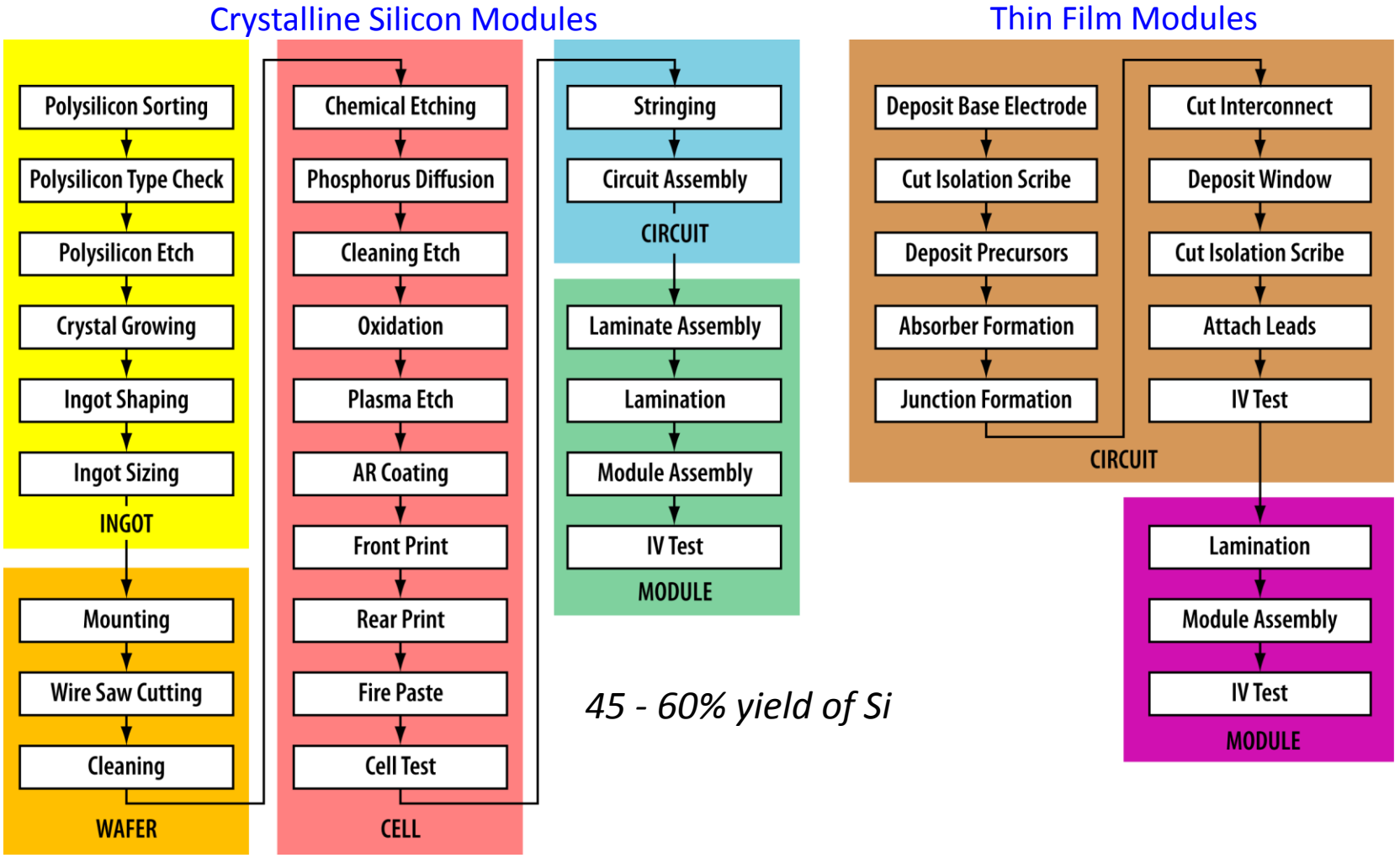
Comparison of Manufacturing Sequence For X-Si and Thin Film

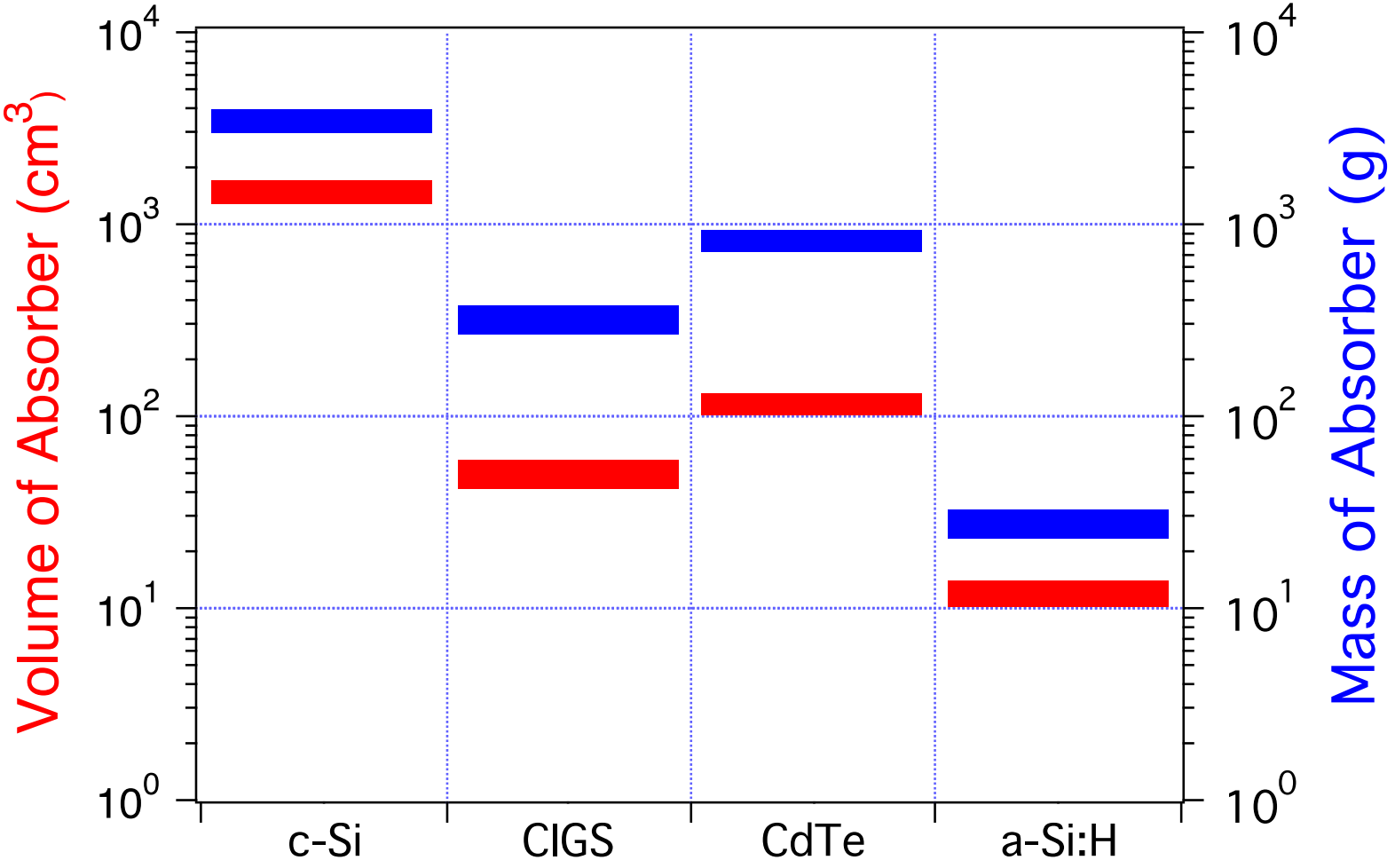
Courtesy of Brian Keyes, NREL



Ref: 'Overview and Challenges of Thin Film Solar Electric Technologies', Harin S. Ullal, Ph.D., NREL 2008

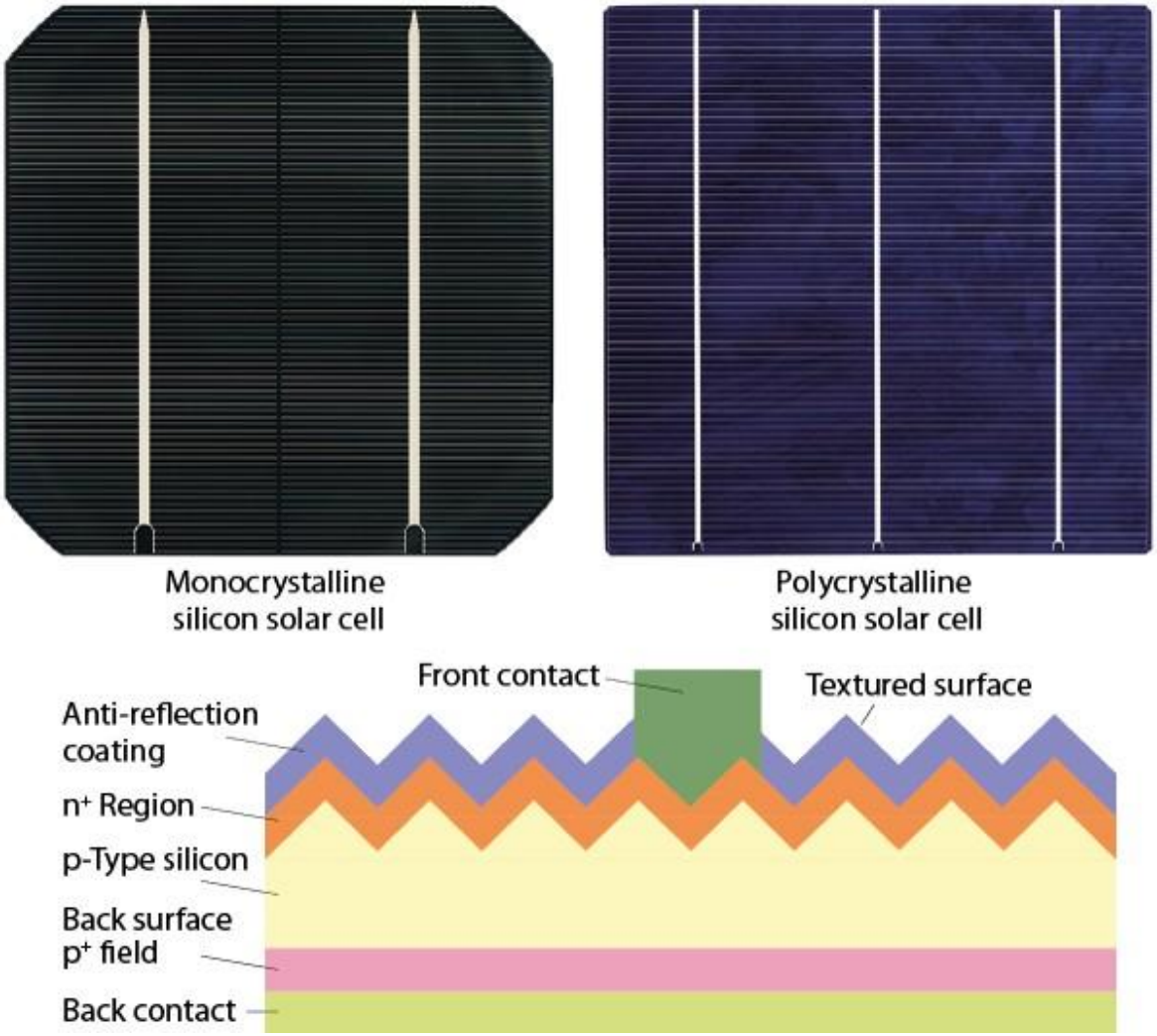
Thin film PV uses less semiconductor material

Courtesy of Brian Keyes, NREL



Amount of material needed for 1 kW output (more area for less efficiency).

“Standard” Silicon PV Cells



Typical mono- and polycrystalline silicon solar cells (upper), and simplified cross-section of a commercial monocrystalline silicon solar cell (lower) (© 2010 Sharp).

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“Standard” Silicon PV Cells (cont.)

- Back-surface p+ field (BSF) regions are formed on the back surface to suppress recombination of minority carriers. The BSF regions are usually formed by firing screen-printed aluminum paste in a belt furnace.

- The minority carriers (electrons) generated in the silicon bulk and diffusion layers are collected by silver contacts (electrodes) formed as gridlines connected by a bus bar to form a comb-shaped structure.

- The back contact is usually an aluminum layer which is connected the adjacent cell via soldered copper or printer silver interconnects.

- The front contact is formed using screen-printed silver paste applied on top of the ARC layer, with “fire through” technology, which also produces the BSF

- The screen-printed front silver contact prepared by firing to penetrate the ARC is one of the most important techniques for large-volume fabrication of modern xstal Si cells.

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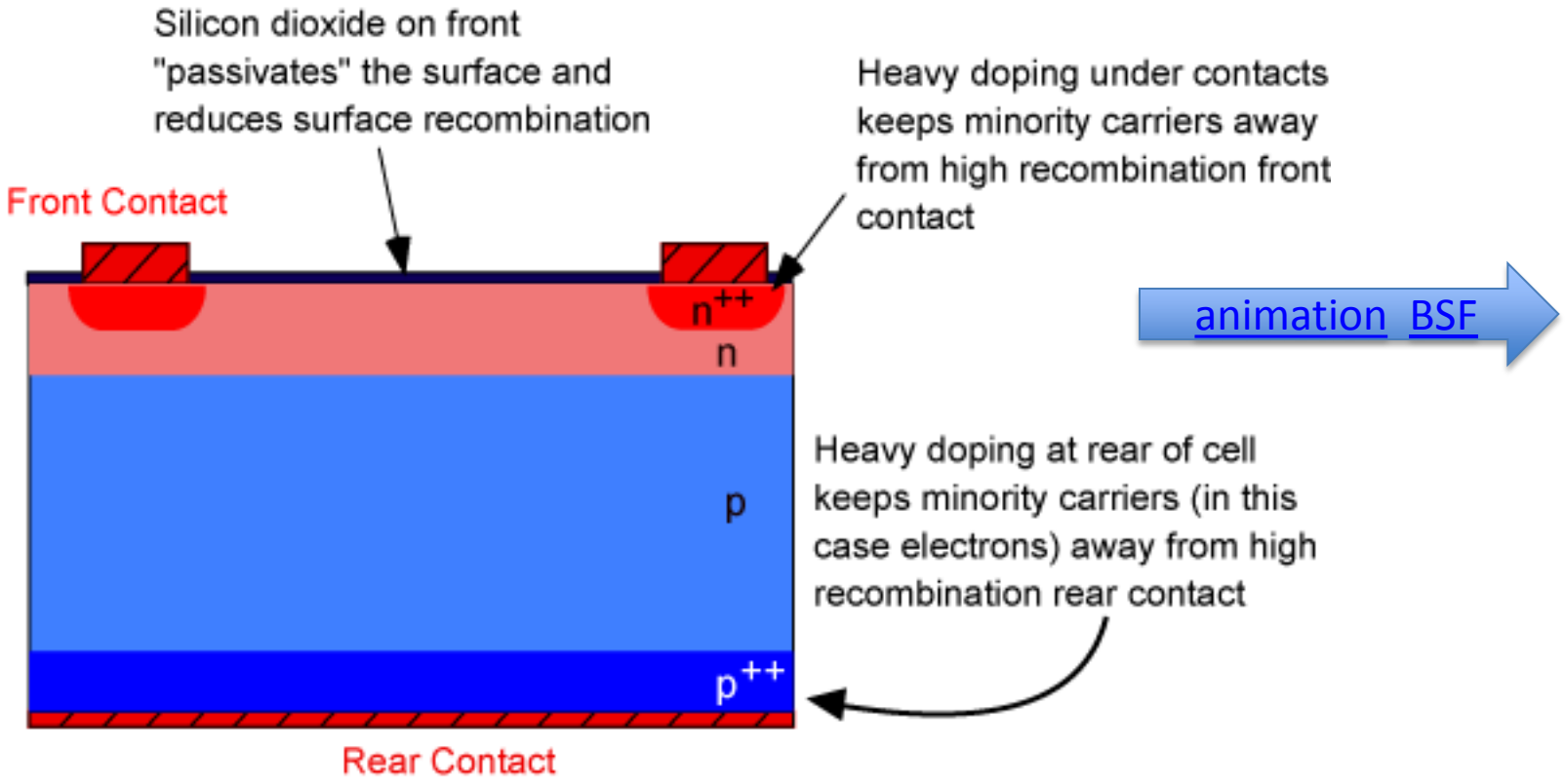
BSF in Silicon PV Cells

Surface recombination can have a major impact both on the short-circuit current and on the open-circuit voltage. High recombination rates at the top surface particularly impact J_{SC} since the top surface generates a high concentration of carriers. Lowering the top surface recombination is typically accomplished by reducing the number of dangling silicon bonds at the top surface by growing a "passivating" layer (usually silicon dioxide) on the top surface. Recombination at the back surface become inreasingly important for thin cells with long minority carrier lifetimes.



http://pvcdrom.pveducation.org/DESIGN/SURF_MIN.HTM

“Standard” Silicon PV Cells

The industrial goal for PV power is to reduce the electricity generation cost to the equivalent of that for commercial grid electricity. The energy conversion efficiency of solar cells is another important issue because the efficiency influences the entire value-chain cost of the PV system, from material production to system installation.

The solar cell efficiency is limited by the three loss mechanisms:

- photon losses due to surface reflection, transmission through c-Si, and back contact absorption;
- minority carrier (electrons in the p-region and holes in the n-region) loss due to recombination in the silicon bulk and at the surface; and
- heating joule loss due to series resistance in the gridlines and busbars, at the interface between the contact and silicon, and in the silicon bulk and diffusion region.

In the design of solar cells, these losses are minimized without lowering the productivity of the solar cells.

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“Standard” Silicon PV Cells

The basic cell structure used in current industrial crystalline solar cells were developed for space and terrestrial use in the 1970s:

- lightly doped n+ layer (0.2–0.3 μm) for better blue-wavelength response
- a BSF formed by a p/p+ low/high junction on the rear side of the cell
- a random pyramid-structured light-trapping surface
- an ARC optimized with respect to the refractive index of the glue used to adhere to it.
- The efficiency of monocrystalline cells for space use is in the range of 14–16% under ‘1 sun’ AM0 test conditions, equivalent to 15–17% at AM1.5.
- These standard structures for crystalline silicon cells are still used in standard industrial crystalline cells, which offer efficiencies in the range of 14–17%.

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Key technologies needed to realize efficiencies > 20% were developed in the 1980s and '90s, and the latest high-efficiency crystalline silicon cells possess most of these features (Table 1).

Table 1. Key technologies for high-efficiency crystalline silicon solar cells

Minimizing carrier loss
Passivation of front electrode (partly in contact with highly doped silicon layer) to reduce carrier recombination under front electrode
Shallow-doped p–n junction with front surface dielectric passivation layer to reduce carrier recombination in the n^+-doped region and at the surface; heterojunction with thin amorphous layers on a crystalline silicon base in a heterojunction cell; front surface field and surface passivation for back contact in a back-junction cell
Locally p^+-doped back surface field and point contact structure to reduce carrier recombination in highly doped p^+ back region
Back surface passivation by a dielectric layer or heterojunction structure to reduce back surface recombination

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Minimizing photon loss
Front textured surface of random pyramid or inverted pyramid structures to reduce surface reflection loss
Single- or double-layer ARC to reduce surface reflection loss
Back-contact cell structure to reduce front contact shadow loss
Flat back surface by chemical etching of silicon to improve back reflectivity and reduce photon absorption
Back surface reflector consisted of a dielectric layer and high-reflectivity thin metal layer to reduce photon absorption

Minimizing electrical loss
Fine gridline front contact to reduce series resistance of n^+-doped region
Selective emitter (deep and highly doped emitter under the contact) to reduce contact resistance of front contact with silicon surface
n-Type or p-type silicon substrates with minority carrier diffusion lengths longer than the base thickness

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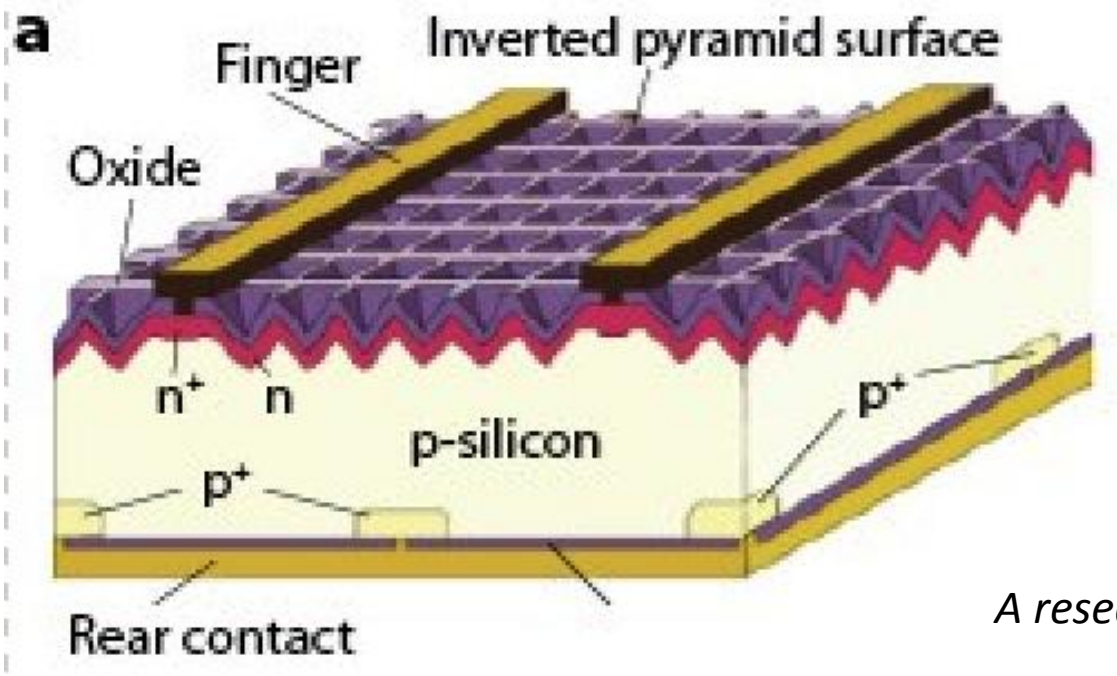
Passivated Emitter Rear Localized (PERL) cell:



A research cell

Front and rear surface passivation, inverted-pyramid light-trapping surface, a rear localized p+ layer (BSF), a double-layer ARC, p-type float zone monocrystalline substrate. The bulk minority carrier lifetime > 1 ms. V_{oc}= *706* mV, J_{SC} = 42.7 mA cm^{-2}, FF = 0.828 and η = 25.0% for a 4 cm^2 cell [4]. J_{SC} is close to limit for absorption/collection in the emitter and base. η= 24.7% was reported almost 10 years ago, and record of 25.0% (University of New South Wales - UNSW) in 2009 was from remeasurement of the same cell. Full PERL design is not easy to apply to low-cost industrial production because of the necessity for multiple photolithography steps. Expensive silicon PV cells for space applications have a similar structure to the PERL cell.

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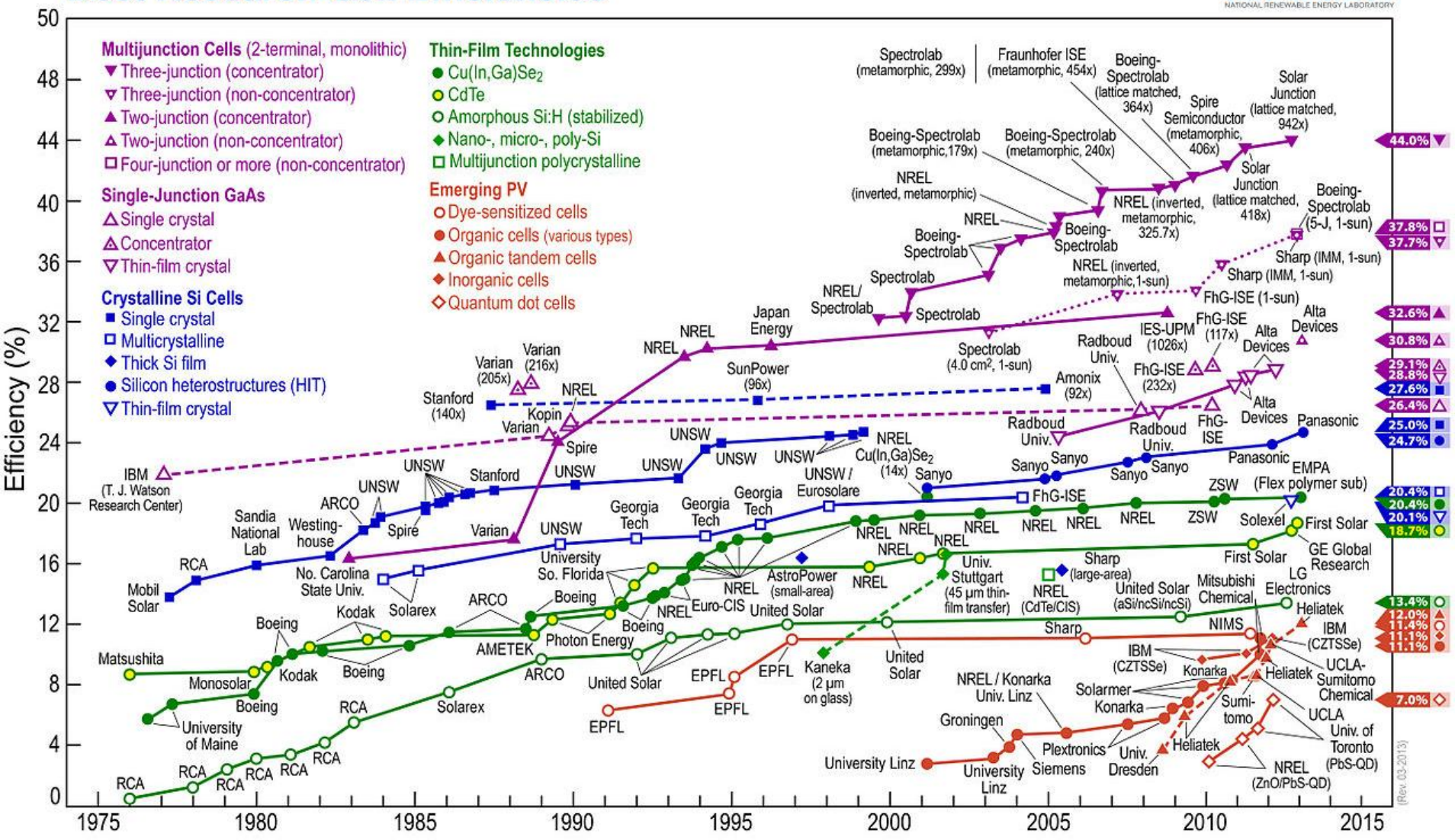
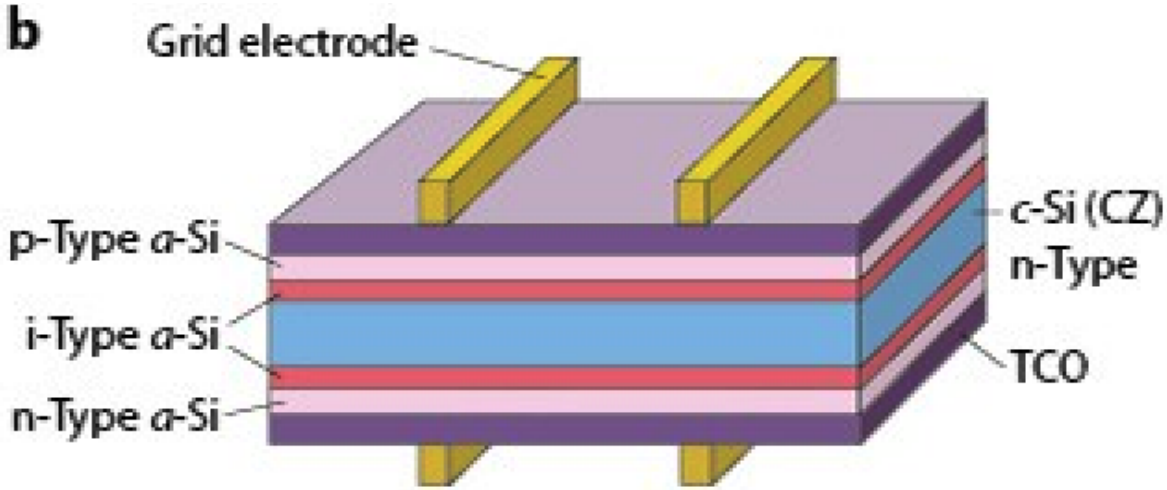
Best Research-Cell Efficiencies

NREL
NATIONAL RENEWABLE ENERGY LABORATORY



Heterojunction with intrinsic thin layer (HIT) cell:



Developed for manufacturing; has thin amorphous p- and n- layers and intrinsic amorphous layers on the front and rear surfaces of a CZ n-type monocrystalline-silicon substrate. Best output parameters are V_{oc} = 729 mV, J_{SC} =39.5 mA-cm^{-2}, FF = 0.800, and η = 23.0% for a large 100.4 cm^2 cell. Voc is improved by large bandgap of the front amorphous silicon layer and the high interface quality between the a-Si and x-Si substrate. Low temperature coefficient of 0.30% K^{-1} at P_{max} is advantage (~0.45% K^{-1} for other x-Si cells). TCO ARC reduces sheet resistivity of front a-Si layers. Lower Jsc in comparison to other high-efficiency Si cells due to weaker blue response. Generation/collection in the front a-Si layers and bulk Si is lower due by the effects of the lower transparency of the TCO layer compared to other ARCs and/or the lower internal quantum efficiency of the amorphous layers.

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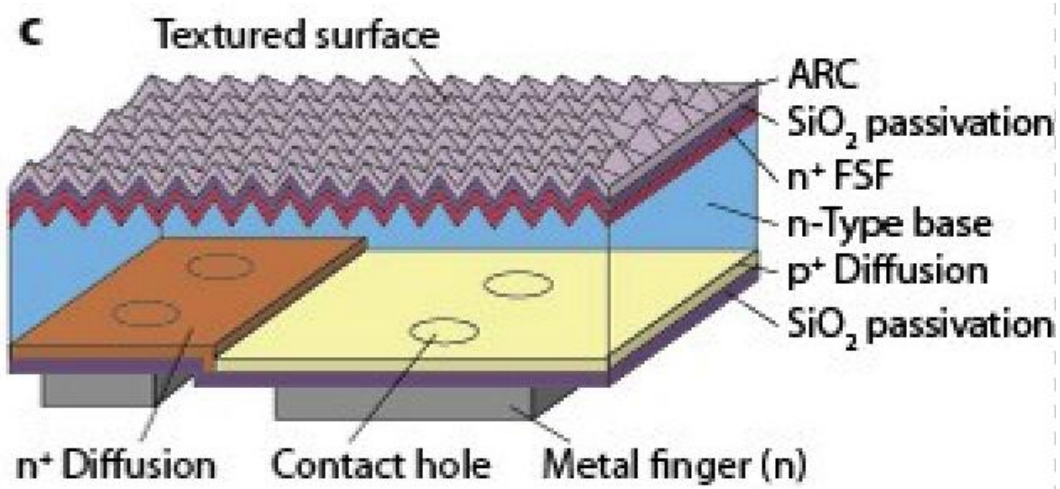
Back Contact Back Junction (BC-BJ) cell:



Interdigitated n- and p-doped regions and n and p contacts on the back surface. Original BC-BJ cell, called the FSF cell or interdigitated back contact (IBC) cell developed for space PV in late 1970s. The BC-BJ-structured point contact (PC) cell developed by Stanford University in the 1980s had η > than 20%. SunPower made BC-BJ cells for unmanned aircraft and solar race cars in the 1990s, followed by large-scale PV plants in 2000s. Best efficiency for a large-area industrial BC-BJ cell is 23.4%. The BC-BJ cell has front and rear surface passivation layers, a random-pyramid light-trapping surface, FSF, interdigitated n- and p-doped regions on the back surface, n and p contact gridlines on n- and p-doped regions, a single-layer ARC and CZ n-type single-crystalline silicon substrate with a minority carrier lifetime > 1 ms. Of all silicon PV modules on market at this time, only those based on BC-BJ cells provide the possibility of module efficiencies exceeding 20%. BC-BJ cells have no gridlines or busbars shading, a front surface with good passivation and improved asthetics due to the absence of front electrodes, which permits freedom in the design of back contacts.

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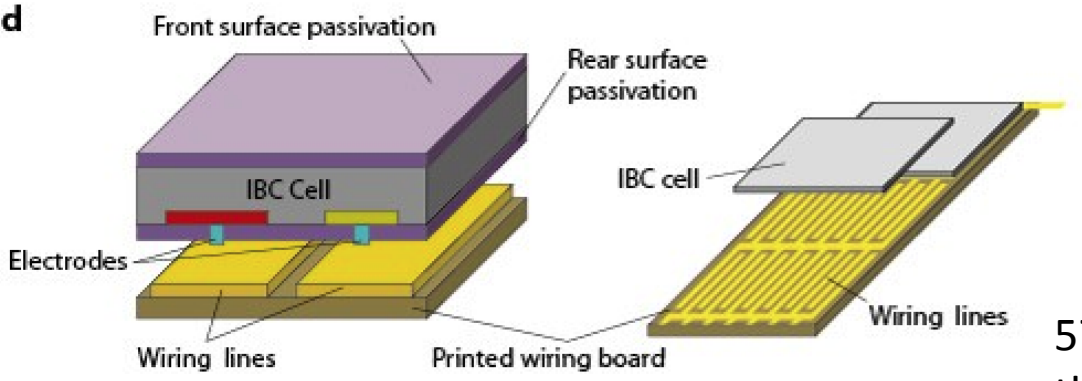


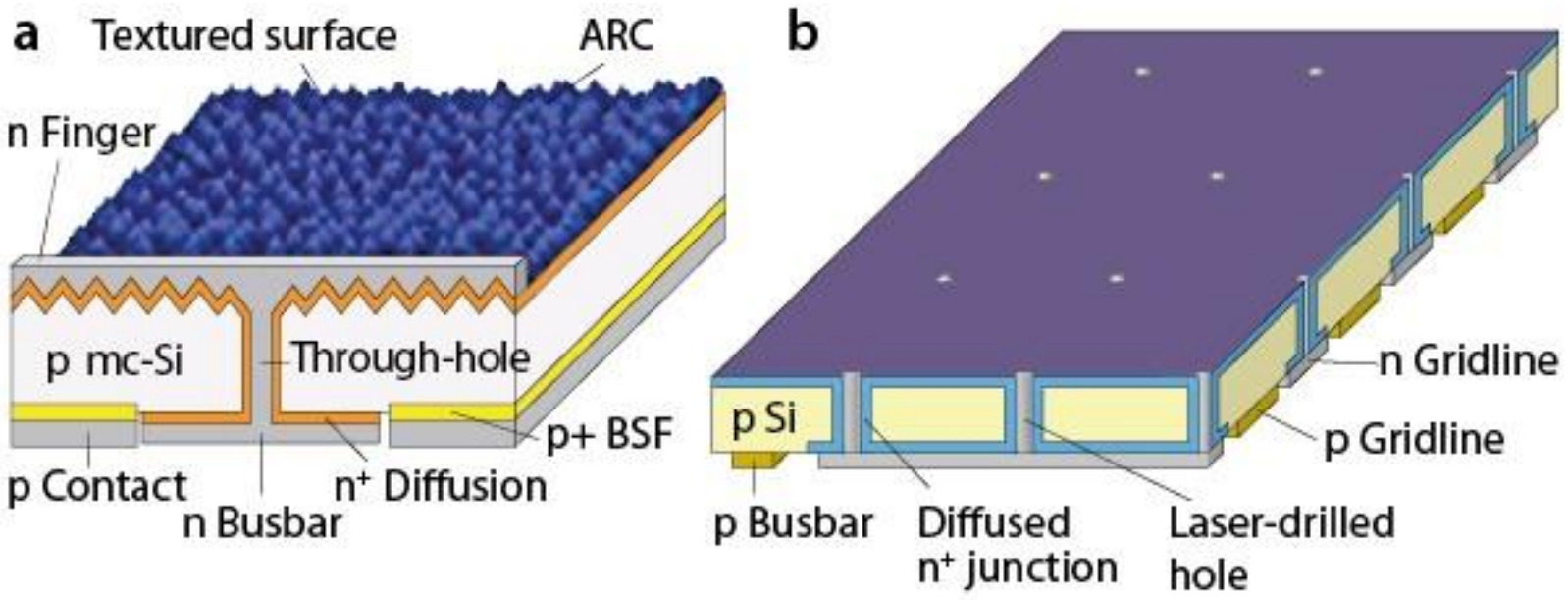
57 K panels, 100 acres, 10 MW, largest in the world when completed in 2004

Freedom in design of back contact also provides advantages in module assembly, allowing the simultaneous interconnection of all cells on a flexible printed circuit. The low series resistance of interconnection formed by this type of surface-mount technology results in a high *FF of 0.80,* compared with around 0.75 for standard silicon PV cell modules.

http://us.sunpowercorp.com/downloads/success-stories/utility/SPWRBavaria_CS_0808.pdf

Emitter Wrap Though and Metal Wrap Through Cells

- Schematics of back-contact solar cell structures. (a) MWT. Adapted from Ref. 26 (© 2008 WIP Munich). (b) EWT. Adapted from Ref. 25 (© 2008 IEEE). All figures reproduced with permission.



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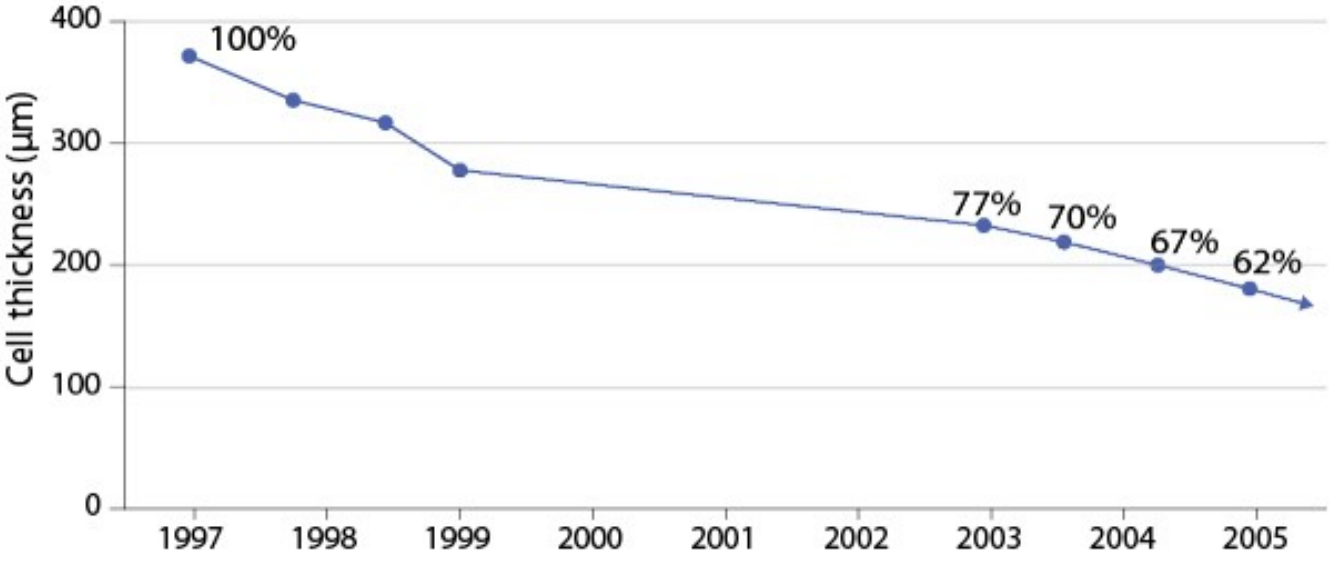
Reducing the amount of Si in the cell, by reducing the silicon wafer thickness (© 2010 Sharp)



c-Si Cell Description: 2030

*Based on publicly disclosed (literature) cell designs, not intended to depict proprietary architectures

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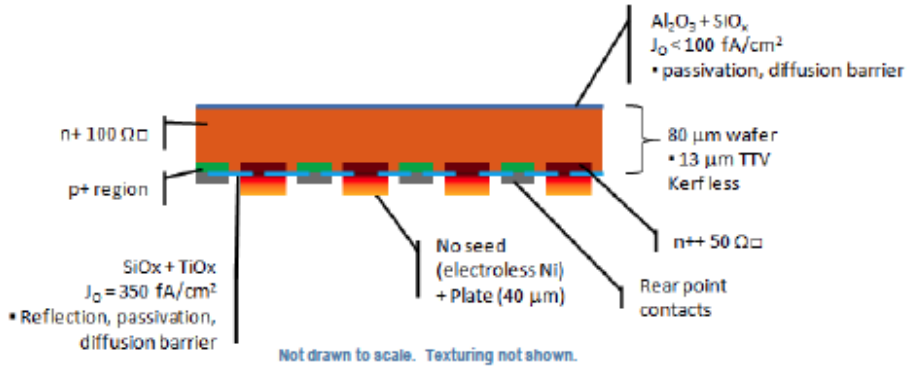
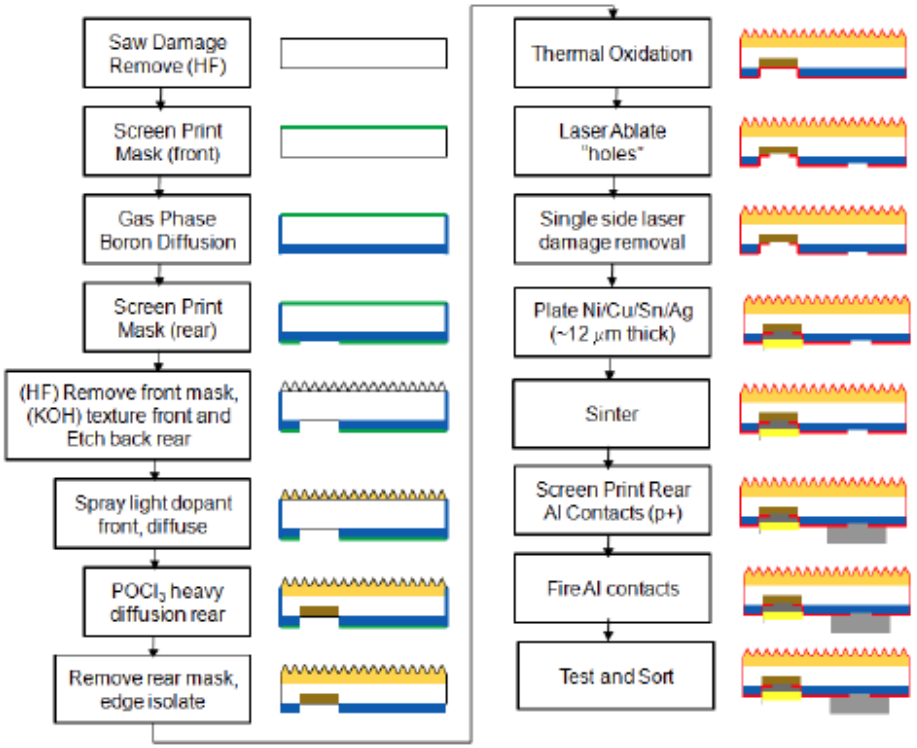


- All Rear (Interdigitated) Contacts
- High lifetime (n- type) wafer
- Ultra thin (80 microns) kerfless wafers
- High quality surface passivation
- Plated emitter contacts
  - Electroless nickel barrier, Cu plating
- Base point contact absorbers
  - Printed Al contacts



ENERGY

Silicon Solar Cells Ditch the Wafers

A startup's silicon solar cells save on costs by using less material.

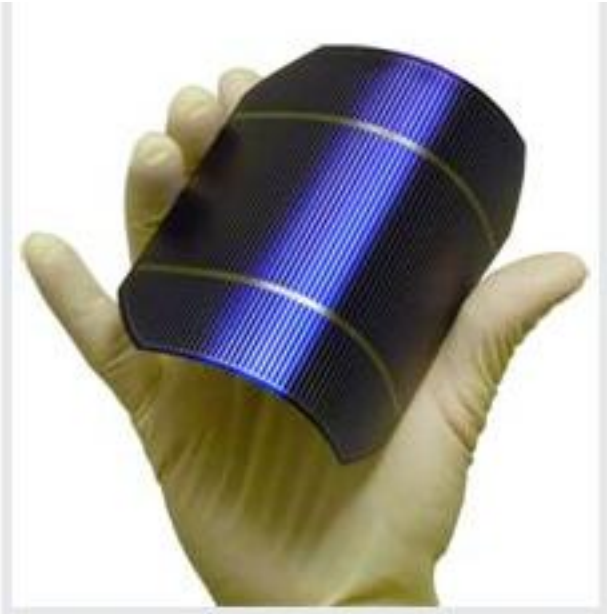
Skinny silicon: These solar modules, made from silicon films just 40 micrometers thick, have a 15 percent efficiency.
Credit: Crystal Solar

ENERGY

Nano Ink Boost for Silicon Solar

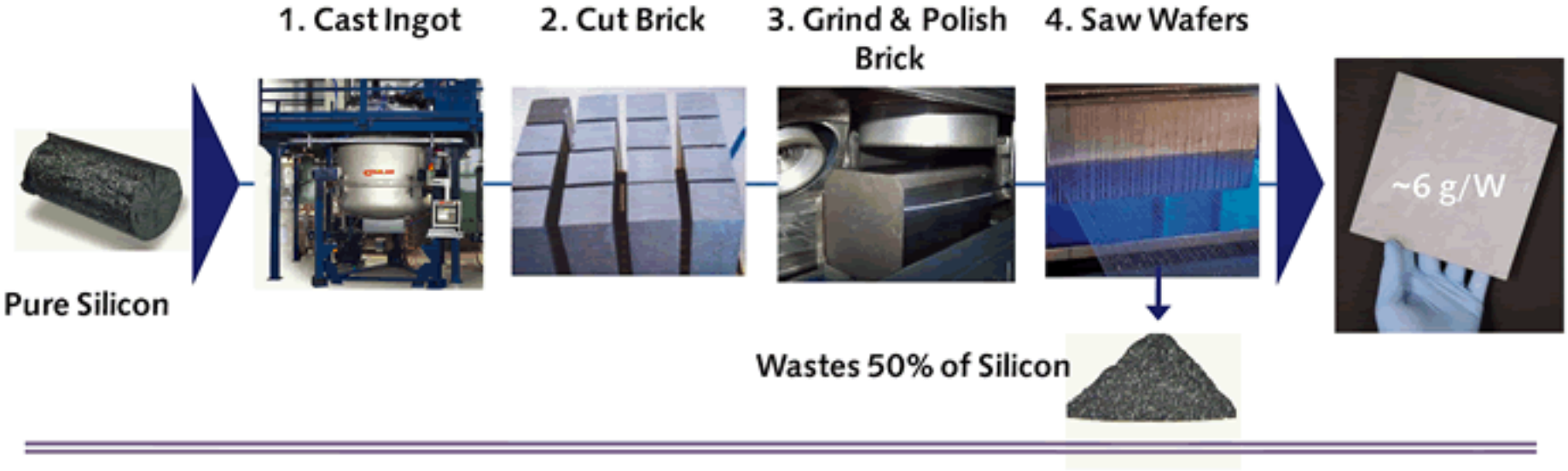
Inkjet-printed silicon increases solar-cell efficiency.

FRIDAY, SEPTEMBER 18, 2009 | BY KATHERINE BOURZAC



Inkjet solar: The inkjet printing process allows Innovalight to make silicon wafers that are thin enough to bend.
Credit: Innovalight

Standard Process



1366 Direct Wafer

Example c-Si modules

SunPower 240:

http://us.sunpowercorp.com/cs/Satellite?blobcol=urldata&blobheader=application%2Fpdf&blobheadername3=Content-Disposition&blobheadervalue3=attachment%3B+filename%3Dsp_e19_240ewh_ds_en_ltr_p_366.pdf&blobkey=id&blobtable=MungoBlobs&blobwhere=1300271294839&ssbinary=true

SunPower X21-345:

http://us.sunpowercorp.com/cs/Satellite?blobcol=urldata&blobheadername1=Content-Type&blobheadername2=Content-Disposition&blobheadervalue1=application%2Fpdf&blobheadervalue2=inline%3B+filename%3DSPR-X21-335%2BSPR-X21-345%2Bdatasheet.pdf&blobkey=id&blobtable=MungoBlobs&blobwhere=1300285947420&ssbinary=true

Isofoton ISF-250:

http://www.isofoton.com/sites/default/files/250-black_en__2.pdf