Understanding the Interplay Between CdSe Thickness and Cu Doping Temperature in CdSe/CdTe Devices

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***Abstract*—CdSe thickness and Cu doping play significant roles in achieving high efficiency in CdTe solar cells. Using an evaporated CdSe/CdTe device stack to avoid vacuum breaks between deposition of layers, we investigated the role of the CdSe thickness on the device performance. When the CdSe thickness was greater than a critical value the device performance suffered primarily due to a reduction in the short-circuit current density (J_{SC}). The critical thickness of CdSe was determined to be 120 nm. However, in some cases the CdSe thicknesses could be increased to larger values by increasing the Cu doping process temperature. The higher temperature process leads to an increase in J_{SC} and an overall improvement in device efficiency. Specifically, for a device with ∼270 nm of CdSe, the J_{SC} increased from 7.9 mAcm^{-2} with $CuCl_2$ processing temperature of 200°C to ∼29 mAcm^{-2} when the processing temperature was increased to 250°C.**

***Index Terms*—CdTe, $CuCl_2$, evaporation, photovoltaics, solar cells.**

I. Introduction

REPLACING the CdS window layer in CdTe-based solar cells with CdSe has been critical to achieving higher efficiency devices. The low solubility limit of CdS in CdTe results in devices with an absorbing layer with poor carrier collection at the front of the device that reduces short-circuit current density (J_{SC}). The high solubility of CdSe in CdTe, on the other hand, can result in complete consumption of the CdSe to form $CdSe_xTe_{1-x}$ alloys during deposition and/or $CdCl_2$ activation [1], [2]. For x less than ∼0.40 the $CdSe_xTe_{1-x}$ bandgap decreases compared with CdTe and remains photoactive [3]. The lower bandgap and removal of the parasitic absorption layer results in much higher J_{SC} values [2], [4]. In addition, inclusion of CdSe leads to passivated grain boundaries and relatively long carrier lifetime in a $CdSe_xTe_{1-x}$ absorber layer [5], [6].

The effect of the CdSe thickness in these devices has been studied and is critically important. Initial investigations in which low temperature (250°C) sputtering was used to fabricate the devices showed that the J_{SC} increased with increasing thickness up to ∼200 nm, and began decreasing with thicker CdSe [2]. Similar results were reproduced by Ablekim *et al.* [7] for devices fabricated by thermal evaporation at 400°C, and the characterization supported that the device performance dropped once x exceeded ∼0.4. It has been shown that at x values >0.4, $CdSe_xTe_{1-x}$ is in wurtzite crystal structure, and the bandgap begins to increase [8], [9]. This wurtzite phase being photoinactive corresponds to the loss in J_{SC} in the $CdSe_xTe_{1-x}$ devices, so the decrease in performance has been attributed to the crystal structure change and accompanying bandgap increase when x was >0.40 [10].

At the same time, the Cu doping process is also critically important to the device performance. Transitioning from using evaporated Cu to a solution processed $CuCl_2$ dopant source led to an increase in the open circuit voltage (V_{OC}) and fill factor [11]. This change in the dopant source needed to be accompanied by a reoptimization of processing time and temperature. The optimized Cu treatment varies for CdTe devices deposited method, absorber thickness, absorber composition, and Cu source material. For our typical 3.5 μm CdTe absorber layer deposited by CSS, Cu diffusion is carried out at 200°C for 20 min, whereas for a 2.1-μm CdTe absorber deposited by sputtering the treatment time is reduced to 15 min at 200°C [12]. Li *et al.* [13], on the other hand, reported a rapid thermal annealing process at 180°C to diffuse Cu from CuCl into ∼3.5 μm CdTe devices deposited by CSS, whereas Munshi *et al.* [4] evaporated CuCl powder to dope CdTe (∼ 4 μm) absorber layer deposited by CSS method by annealing the device at 220°C for 220 s. Clearly, the Cu doping process is quite important; however, there is little discussion in the literature about how it should be modified as research has moved from CdS/CdTe devices in which the near complete active absorber is CdTe to CdSe/CdTe devices in

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which a significant portion of the absorber at the front interface is $CdSe_xTe_{1-x}$.

Here, we investigate the effect of CdSe thickness and Cu doping processing on CdTe solar cells. Devices were fabricated by evaporating a CdSe/CdTe bilayer without exposure to air between the CdSe and CdTe depositions. When the CdSe layer thickness is less than 100 nm, the resultant graded $CdSe_xTe_{1-x}$ film exhibits a bandgap of greater than 1.39 eV and does not absorb long wavelength photons, thus these devices have lower J_{SC} than the device with optimum CdSe thickness. When the CdSe layer thickness is 200 nm or greater, the graded absorber layer still has a minimum band gap of 1.39 eV, but the J_{SC} is low, suggesting an optimal CdSe thickness close to 120 nm. However, increasing the temperature of the $CuCl_2$ doping process results in increased J_{SC} values of $\sim$29 mAcm^{-2} for devices with $\sim$270 nm of CdSe, indicating previous explanations for the J_{SC} loss were incomplete.

II. Experimental

Bilayer CdSe/CdTe solar cells were fabricated on fluorine doped tin oxide coated glass substrates with a 50-nm thick dopant-free tin oxide layer on the surface (TEC^{TM} −12D, NSG Pilkington). CdSe and CdTe films were deposited sequentially by evaporating CdSe and CdTe powders (99.999%, Alfa Aesar) with a substrate temperature of 400°C and a base pressure of 4×10^{-6} Torr at deposition rates of $\sim$15 and $\sim$100 nm-s^{-1}, respectively. The time between CdSe and CdTe depositions was $\sim$3 min, during which the substrate temperature was maintained at 400°C. After deposition and cooling, the CdSe/CdTe stacks were activated with $CdCl_2$ using a saturated $CdCl_2$ solution in methanol. Four to five drops of $CdCl_2$ solution were placed on the a CdTe surface (1.5" × 1.5") and the device stack was annealed at 400°C for 30 min in dry air, followed by two rinses with methanol and drying with nitrogen. Then, 0.1 mM $CuCl_2$ solution in deionized water was used for Cu activation as reported previously [14]. For the set of experiments in which the CdSe thickness was varied, device stacks were heated at 200°C for the Cu treatment in a convection oven. For the set of experiments investigating how the doping processing affected the devices, the treatment temperature was varied from 200°C to 260°C. The duration of all $CuCl_2$ thermal treatments was 20 min in the oven in ambient air. Finally, devices were finished with 40 nm of thermally evaporated gold using a tungsten boat at a base pressure of $\sim 4 \times 10^{-6}$ Torr. A cell area of 0.08 cm^2 was defined using a shadow mask during Au deposition.

Current density-voltage (J-V) characteristics were measured under a simulated AM1.5G spectrum and external quantum efficiencies (EQE) were measured using PV Instruments system (model IVQE8-C). The XRD diffraction patterns of the films were taken using a Rigaku Ultima III X-ray diffractometer with a Cu source operating at 40 KV and 44 mA. The surface morphology of the CdTe films was studied using a Hitachi S-4800 scanning electron microscope (SEM).

III. Results and Discussion

Prior to completing devices, we investigated the crystal structure and morphology of as-deposited and $CdCl_2$-activated

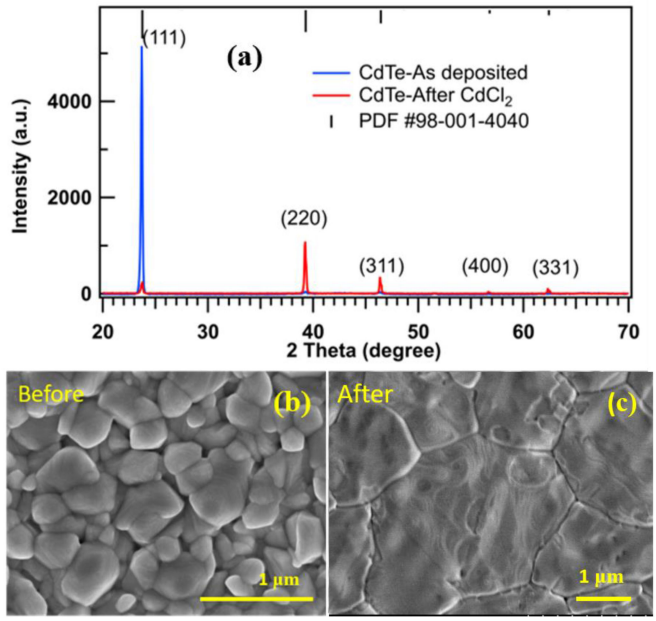

Fig. 1. (a) X-ray diffraction pattern and surface scanning electron micrographs of CdTe films (b) before and (c) after $CdCl_2$ treatments. The vertical lines (black lines, top scale) are diffraction patterns for CdTe (PDF #98-001-4040).

devices. Fig. 1 shows the XRD and SEM images of these samples. From the XRD data, we see that the as-deposited film has grains with preferred orientation along (111) plane, whereas after $CdCl_2$ treatment the film has more randomly oriented grains [15]. The XRD pattern for as deposited film is consistent with thermally evaporated CdSe [16] and low temperature deposition of CdTe [17]. The $CdCl_2$ process is a critical step in the fabrication of CdTe devices and is known to result in recrystallization [15]. The change in XRD pattern shows the recrystallization.

The SEM images show the growth of the CdTe grains, which is common in low temperature processed CdTe films such as sputtered films [18], [19]. The grains grew from 100–500 nm before activation to 1–3 μm after [see Fig. 1(b) and (c), respectively] after $CdCl_2$ activation process. Also visible in the SEM images are surface features that result due to the $CdCl_2$ treatment which are most likely related to cadmium oxides and/or chlorides [20]. The CdTe grains are in the range of 1–3 μm beneath these oxy-chloride particles on the surface for evaporated films after the $CdCl_2$ treatment visible in Fig. 1(c) after an acid etch. We note that the grain sizes obtained here are comparable to the film thickness, as is the case for films made with higher temperature techniques such as CSS or VTD [21], [22].

The large grains after $CdCl_2$ treatment suggest that these evaporated film stacks have the potential to make high efficiency devices. To verify this, we completed the devices and measured the photovoltaic response. Fig. 2 shows J-V, EQEs, and d(EQE)/dλ of CdTe devices with various CdSe thickness ranging from 40 to 400 nm. For all the devices, $CdCl_2$ treatments were carried out at the same temperature (400°C) and time (30 min) in dry air. For low temperature deposition processes, such as evaporation, as-deposited samples have higher CdSe concentration at the front interface [7], and during the $CdCl_2$ treatment the CdSe

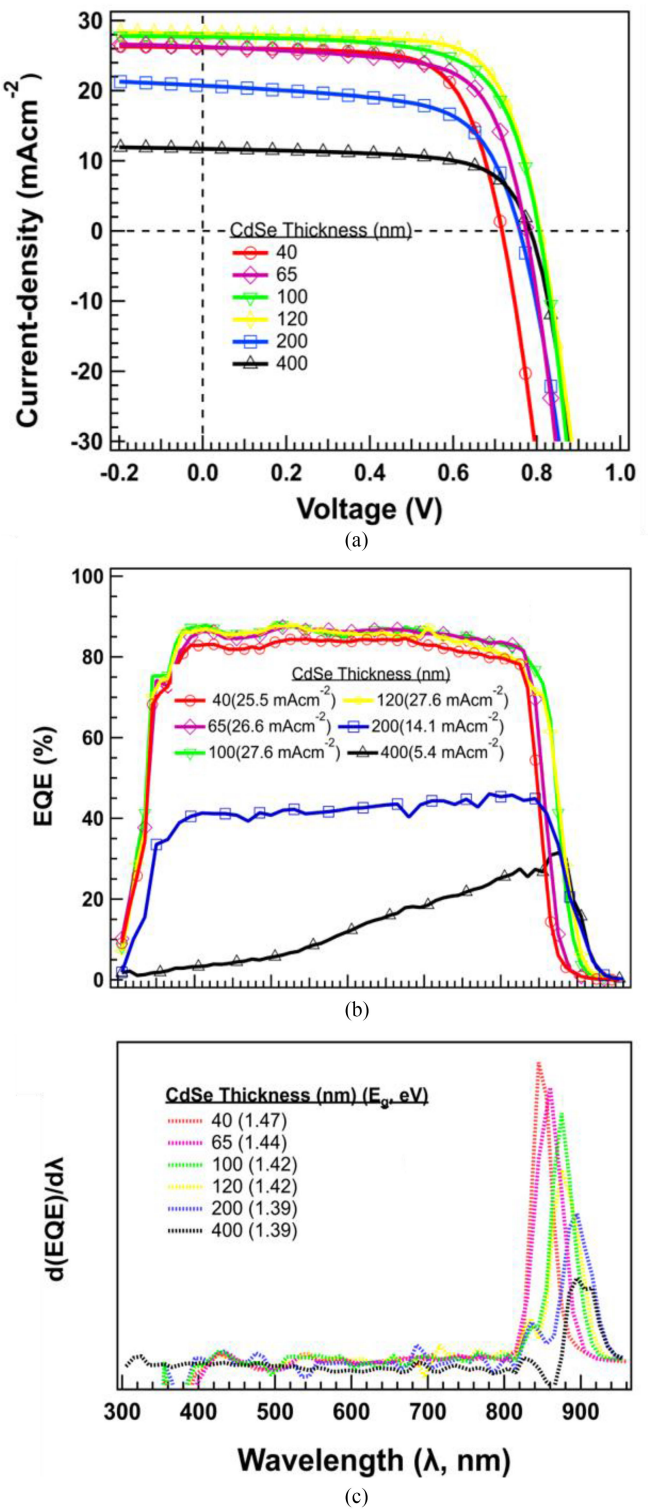

Fig. 2. (a) J-V, (b) EQE, and (c) d(EQE)/dλ data for devices with different CdSe thicknesses. The devices were $CdCl_2$ treated at 400°C for 30 min in dry air and $CuCl_2$ treated at 200°C for 20 min.

alloys with CdTe to form a graded $CdSe_xTe_{1-x}$ film with varying band gap [1]. The composition of this layer is important to the device performance.

Fig. 2(a) shows the J-V characteristics of the CdSe/CdTe devices with varying CdSe thickness, and Table I shows the tabulated PV parameters. For a device having CdSe thickness less than 100 nm, the J_{SC} values obtained from J-V measurements are lower than the devices with CdSe thickness of 100–120 nm. As the thickness of CdSe increases to 200–400 nm, the J_{SC} values drop significantly. The J_{SC} value of ∼28 mA-cm^{-2} refers to the optimum band gap to absorb long wavelength photons by the formation of $CdSe_xTe_{1-x}$ absorber layer with a band gap close to 1.4 eV [3], [23]. The overall device performance, including FF and J_{SC}, depends on several factors including the band gap of the graded $CdSe_xTe_{1-x}$ absorber layer, $CdCl_2$ treatment and Cu doping, and the efficiency strongly followed the variations in J_{SC} values.

To explain these variations, we turn to the EQE response [see Fig. 2(b)]. For the device with 40 nm CdSe, the EQE curve in the long wavelength region (>800 nm) starts dropping at ∼825 nm, which is similar to a typical CdS/CdTe devices [24], indicating a low concentration of Se in the $CdSe_xTe_{1-x}$ layer resulting in little change in bandgap from that of CdTe [12]. For the devices with CdSe thickness >100 nm, the long wavelength edge of the EQEs increases to ∼845 nm, indicating the formation of alloyed $CdSe_xTe_{1-x}$ layer with a lower band gap.

To extract the energy band gaps of these $CdSe_xTe_{1-x}$ films, d(EQE)/dλ was calculated [see Fig. 2(c)]. This graph clearly shows the variation of band gaps of $CdSe_xTe_{1-x}$ layer. The bandgaps range from 1.47 to 1.39 eV for 40 to 400 nm CdSe layer. For a 40 nm CdSe, the bandgap obtained here (1.47 eV) is similar to the band gap of pure CdTe (1.48 eV) [25]. The integrated J_{SC} values obtained from the EQEs for the 100 and 120 nm CdSe layers are the same, as are the minimum band gap values obtained from d(EQE)/dλ graphs. At the same time, for the devices with CdSe layers of 200 and 400 nm, the minimum bandgap is not much larger. In this case, the $CdSe_xTe_{1-x}$ could form an alloy with a maximum x greater than 0.4, resulting in a wurtzite structure material [23], [26] that is not photoactive and has an increased bandgap at the front interface [27]. Thus, a portion of the graded alloy is inefficient in collecting absorbed photons. Since a large portion of the incident photons are not able to reach the more effective portion of the absorber layer, the J_{SC} values are low (14.1 mAcm^{-2} and 5.4 mAcm^{-2}, respectively, for devices with 200 and 400-nm CdSe thickness). The J-V and EQE results presented here are consistent with what others have seen [7], [10], as are the explanations [8], [9].

Based on these J-V and EQE results, a CdSe thickness of 100–120 nm is optimal when a 3.5 μm CdTe layer is overlaid, a $CdCl_2$ activation temperature of 400°C for 30 min is used and annealing for Cu doping is done at 200°C for 20 min. While the shape of the EQE can be rationalized as previously noted [7], [10], it is not the only potential explanation. This shape is also reminiscent of back illuminated CdTe devices [28]. In those cases, the junction is far from where the short wavelength carriers are generated, which typically leads to poor collection of the short wavelength devices and higher collection of carriers generated closer to the junction by the long wavelength photons [29].

For that to be the case here, the junction would have to be at the back interface. This could only happen if the absorber is *n*-type. As-deposited CdSe is *n*-type with a band gap of 1.74 eV

TABLE I
PV DEVICE PARAMETERS OF CDSE/CDTE SOLAR CELLS WITH VARYING CDSE THICKNESS (40–400 NM) AND CDTE 3.5 MICROMETERS (ACTIVE DEVICE AREA 0.08 cm^2)

CdSe Thickness (nm)	Minimum Band gap of $CdSe_xTe_{1-x}$ (eV)	V_{OC} (mV)	J_{SC} ($mAcm^{-2}$)	FF (%)	Eff. (η%)	Rs ($\Omega\ cm^2$)	Rsh ($\Omega\ cm^2$)
40	1.47	717	26.2	68.3	12.8	4.5	1399
65	1.44	774	26.3	66.6	13.6	4.3	588
100	1.42	808	28.4	68.7	15.8	3.9	1393
120	1.42	808	28.2	70.6	16.1	2.3	947
200	1.39	759	20.7	62.6	9.8	6.4	339
400	1.39	784	11.7	66.3	6.1	7.3	999

with wurtzite (hexagonal) structure [30]. At higher values of x in $CdSe_xTe_{1-x}$ (CST), the crystal structure is also wurtzite and has shown to be *n*-type, [26] so it is possible $CdSe_xTe_{1-x}$ in our case is also *n*-type prior to Cu doping. This possibility, and the fact that addition of CdSe to the absorber may alter how the doping occurs during processing, necessitating more aggressive doping.

To test if this is the case, we varied the Cu doping process temperature for the devices. We deposited a thick CdSe layer (∼270 nm) followed by 3.5 μm CdTe on a 3" × 3" substrate, which was then cut into pieces (1" × 1") for the Cu doping study. For this, we varied the temperature of the doping process from 200°C to 260°C. The resultant EQEs and J-V curves are shown in Fig. 3. As abovementioned, the low temperature processing resulted in low J_{SC} with short-wavelength light not being collected. As the annealing temperature increases, J_{SC} increases, with a significant gain occurring when the device was annealed for 250°C for 20 min. The EQE graphs show that the triangular shape observed for 200°C changes to a square shape at the higher temperatures. The EQEs for devices annealed at 250°C and 260°C have very similar shapes to each other, and the J_{SC} values are close (29.2 $mAcm^{-2}$); however, the device annealed at 260°C suffers from a reduction in FF. For the device annealed at 250°C has the highest device efficiency of 15.2% with V_{OC} 780 mV, FF 68.0%, and J_{SC} 28.7 $mAcm^{-2}$.

It is possible that the higher temperature alone could have affected the device performance independent of the Cu. To test this, we heated a Cu-free sample to 250°C for 20 min, then completed a $CuCl_2$ treatment at 200°C for 20 min and completed the device as abovementioned. The EQE curve of this device is shown in Fig. 3(b). We observed some improvement in EQE response in long wavelength region compared with other devices annealed at a temperature ≤240°C; however, the device still has the triangular shape EQE curve. This response indicates that the improvement in device performance observed for samples Cu treated at 250°C is not simply the effect of annealing. Instead, it is the effect of aggressive Cu doping for a device with thicker CdSe.

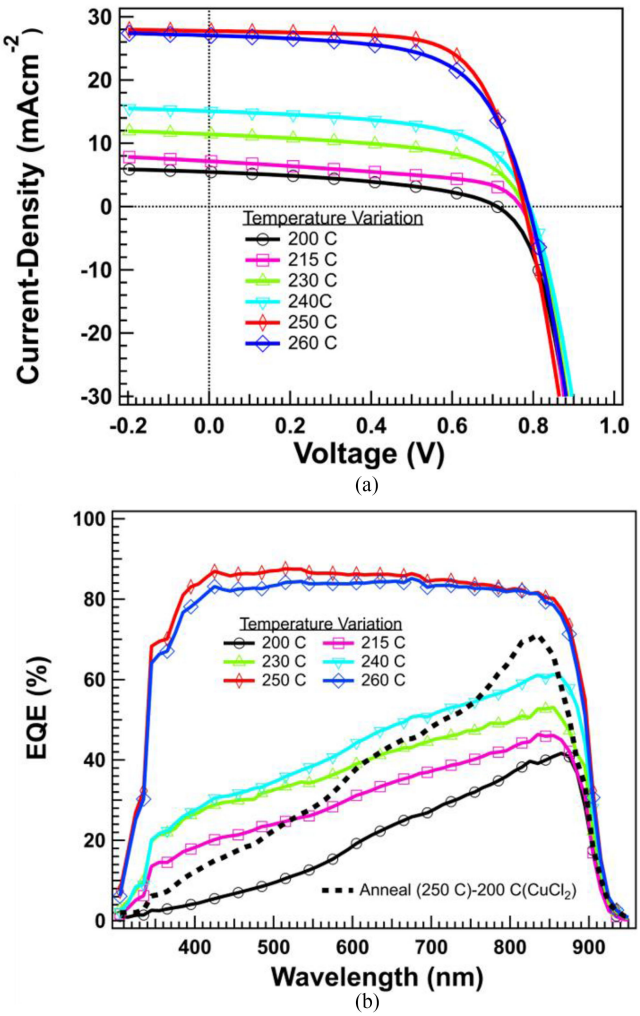

Fig. 3. (a) J-V and (b) EQEs of CdSe/CdTe devices (CdSe thickness 270 nm) with varying annealing temperature as indicated for 20 min. The dotted black line represents an EQE of a device which was first annealed at 250°C, dipped in $CuCl_2$ solution, and then annealed at 200°C for 20 min. All the devices have same $CdCl_2$ treatment at 400°C for 30 min in dry air environment.

This evolution of J_{SC} and EQEs as the annealing temperature increased indicates incomplete Cu doping occurred for devices processed at the low temperatures. These results clearly show that the CdSe thickness alone does not fully explain the reduced J_{SC} for CdSe/CdTe devices and that the thermal budget during the entire device processing of CdSe/CdTe is important.

V. Conclusion

Here, we successfully fabricated CdSe/CdTe devices by thermal evaporation and studied the effect of CdSe thickness on device performances. The CdSe thickness in the range of 100–120 nm produces a high J_{SC} when the devices undergo $CdCl_2$ activation at 400°C for 30 min. Very thin CdSe was not enough to significantly change the band gap of the $CdSe_xTe_{1-x}$ layer from the CdTe value. A thick ($\geq$200 nm) CdSe layer, on the other hand, leads to a decrease in J_{SC} typically thought to be due to a $CdSe_xTe_{1-x}$ layer that is partially nonphoto responsive and absorbs incident photons before reaching the photoactive absorber layer. However, increasing the Cu doping process temperature can result in an increase in J_{sc} (29 $mAcm^{-2}$) for some CdSe thicknesses that lead to poor J_{SC} at lower Cu doping temperature.

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