Selective Cd Removal from CdTe for High Efficiency Te Back Contact Formation

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***Abstract* — The presence of a Te-rich surface or an elemental Te layer is beneficial for the formation of a low-barrier back contact for high efficiency CdTe solar cells. Etching processes are widely used to form Te-rich CdTe surfaces while deposition processes such as evaporation are used to form elemental Te layers. Here, we show that a reaction between methylammonium iodide (CH_3NH_3I, MAI) and CdTe can be used to simply and controllably produce elemental Te over a wide processing window. Both X-ray diffraction and Raman spectroscopy confirmed the formation of a Te layer. The MAI-produced Te layer reduces the Schottky barrier height, improves the open circuit voltage (V_{OC}) and fill factor (FF), and outperforms contacts formed with evaporated Te. We examined the effect of MAI reaction temperature and the amount of Cu needed to optimize the device. CdS/CdTe stacks that were treated with a 125 mM MAI solution and heated to 125 °C for 10 minutes showed the best power conversion efficiency (PCE) of 14.1%, while the best efficiency of a standard device without treatment was 13.0%, and the best PCE of an evaporated Te layer was 13.8%. Notably, the improved efficiency for the MAI-treated devices was achieved with less Cu than was required for the standard device. With an indium tin oxide (ITO) back electrode the PCE was also improved from 11.0% to 12.2% with MAI treatment, providing a potential route for fabricating high efficiency transparent or bifacial CdTe solar cells.**

***Index Terms* — CdTe, Te layer, Schottky barrier, back contact, methylammonium iodide, bifacial, perovskite.**

I. Introduction

CdTe solar cell technology is one of the most well-established approaches for preparing high efficiency, low cost, and stable thin films photovoltaics (PV) [1]. With a direct band gap of 1.45 eV, CdTe is an ideal absorber material for single junction solar cells. A power conversion efficiency (PCE) as high as 22.7% has recently been achieved [2]. Creating an efficient and stable back contact is necessary to fabricate high efficiency CdTe solar cells that exhibit long-term stability [3]. Since CdTe has a high electron affinity, a high work function metal is required to form a low resistance ohmic contact; however, no inexpensive metals have a work function high enough to form an ohmic contact with p-type CdTe. Therefore, CdTe/metal junctions typically produce a Schottky barrier that has a significant contact resistance which causes lower device performance [3-7]. A typical method to reduce the back contact barrier height is to add Cu to the back surface. The added Cu diffuses into the CdTe, producing a p^+ region at the back surface [8, 9] and, when Te is present, a degenerate Cu_xTe semiconductor layer may be formed, depending on the reaction temperature [7, 10-13]. Recently, a Te layer had been shown to produce good device performance even without the use of added Cu [13, 14].

The Te-rich surface is typically prepared by wet-chemical etching processes that may include a dilute solution of bromine in methanol (Br:MeOH) [3] or a mixture of nitric and phosphoric acid in water (NP) [15]. Dry etching is also possible using, for example, an Ar plasma [16]. Alternatively, physical vapor deposition processes such as close space sublimation (CSS) [17] or evaporation [14], or chemical bath deposition (CBD) [18] may be used to form a Te-rich or elemental Te layer on the CdTe absorber.

We recently introduced a new wet process that capitalizes on the ability of organocations such as methylammonium to form low-dimensional Cd-I perovskite structures [19]. In that study, we showed that MAI thin films, which were fabricated on CdTe surfaces by spin-coating MAI/isopropanol (IPA) solutions, could be reacted with the CdTe surface to selectively extract Cd and leave behind a thin elemental Te layer. The process offers facile preparation, reduced toxicity, and high controllability in comparison to both other wet and dry etching processes. Current density-voltage (J-V) characteristics showed significant improvements in open circuit voltage (V_{OC}) and fill factor (FF) when the MAI treatment was employed. We reported the effect of MAI concentration and reaction time on the surface morphology, structure, and device performance with a reaction temperature of 150 °C, [19] and demonstrated an improved PCE (13.5%) for the MAI-treated devices relative the value (12.7%) for standard devices prepared without the treatment.

Here, we explore how the device performance depends on the amount of diffused Cu and the reaction temperature. The PCE for the CdTe devices was increased to 14.1%, and temperature-dependent J-V measurements were used to develop an understanding of the current transport at the back interface. The MAI treatment was also found to be useful for preparing CdS/CdTe solar cells with transparent indium tin oxide (ITO) back electrodes. The Schottky barrier height at the back contact for both Au and ITO electrodes was dramatically reduced with the MAI treatment.

II. Experimental Details

A. Device Stack Preparation

CdS and CdTe were deposited onto soda lime glass substrates having a transparent conducting oxide stack (~500 nm of F:SnO_2, ~100 nm of SnO_2, i.e. TEC 12D) using a commercial vapor transport deposition process [20]. The CdS and CdTe thicknesses were ~200 nm and ~3.0 µm. Note that the material stack was not optimized for device efficiency. Devices in each of the studies reported here came from materials that were deposited near the center of a 60 cm x 120 cm plate that was produced by the manufacturing process. $CdCl_2$ was deposited on the CdTe film using a dropper filled with a saturated methanolic solution. Samples were heated at 387 °C in dry air for 30 min to activate the material [21]. Excess $CdCl_2$ was removed by thorough rinsing with methanol. The MAI treatment was performed by covering the CdTe surface with 500 µL of 125 mM MAI solution in anhydrous IPA. After letting the solution sit on the CdTe layer for 40 s, the sample was spun at 4000 rpm for 20 s to form a thin MAI film on the CdTe surface. The samples were then reacted at 110 °C, 125 °C, 150 °C or 175 °C for 10 min by placing the samples on a hot plate in glove box, followed by thorough rinsing using anhydrous IPA. The 125 mM concentration and 10 min reaction time were chosen from our previous optimization study [19].

B. Film Characterization

X-ray diffraction (XRD) patterns of the films were recorded from 2θ = 20° to 50° with a 0.02° step size and a scanning speed of 0.5°/s using a Rigaku Ultima III X-ray diffractometer. Surface scanning electron microscope (SEM) images of the films were obtained using a field emission scanning electron microscope (Hitachi S-4800).

C. Solar Cell Fabrication

After reacting the MAI thin films with the CdTe surface and rinsing with IPA, different Cu thicknesses (from 0.5 to 5 nm) and 40 nm of Au were deposited by thermal evaporation without breaking the vacuum. The samples were then heated in air at 150 °C for 45 min. Individual cells were formed on a 3 mm x 3 mm grid by laser scribing [22]. The active area of the fabricated solar cells was 0.08 cm^2. For the devices with a transparent back electrode, the Cu diffusion was completed prior to the deposition of 125 nm of ITO by sputtering from a 3" target (Lesker) at room temperature (Ar pressure of 3 mTorr, 100 W power).

D. Solar Cell Characterization

J-V characteristics were measured using a Keithley 2440 digital source meter and a solar simulator (Newport model 91195A-1000) configured to simulate AM1.5 illumination. A NIST-traceable Si reference solar cell was used to calibrate the light intensity. Average values were reported from measurements of at least 20 cells.

E. Low Temperature J-V Measurements

For low temperature J-V measurements the devices were placed in a closed-cycle helium cryostat, and the temperature was varied from 180 to 300 K. A LabVIEW program interfaced to the temperature controller and a Keithley 2400 source-meter allowed for automatic data acquisition. Dark J-V curves were collected while scanning from -0.5 to +1.5 V at 0.01V/s.

III. Results and Discussion

A. XRD Spectra

XRD was used to investigate the effect of MAI treatment on the CdTe back surface. All of the XRD spectra presented in Figure 1 show the three main diffraction peaks for cubic CdTe at 2θ of 23.8°, 39.3°, and 46.4°, corresponding to diffractions from the (111), (220), and (311) crystalline planes, respectively [23].

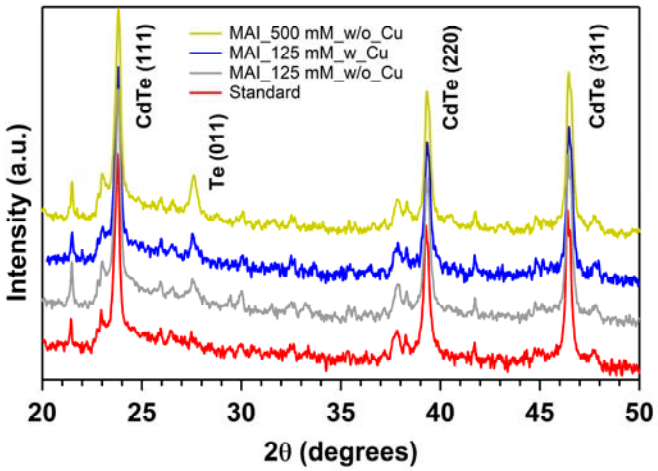

Fig. 1. X-ray diffraction patterns from MAI treated samples using a 125 mM (with and without Cu diffusion) and a 500 mM MAI (without Cu diffusion) solutions, and untreated standard (without Cu diffusion) CdS/CdTe samples.

The MAI-treated samples additionally show a new XRD peak at 27.5°. As confirmed by Raman spectroscopy [19], this peak is due to diffraction from the (011) planes of hexagonal Te, indicating that the MAI treatment selectively removes Cd from the surface. Previously, we showed that the Te signal can be produced over a range of MAI concentrations (125 – 500 mM), and that the thickness of the Te layer is insensitive to the concentration used [19]. The data in Figure 1 also shows that the deposition of Cu followed by a heat treatment does not significantly affect the Te diffraction peak.

B. Surface Morphology

To examine the impact of 125 mM MAI treatment on the morphology of the CdTe surface, scanning electron

microscopy was performed. Figure 2a shows the compact, relatively large grains after $CdCl_2$ treatment. After MAI treatment, the CdTe surface is conformally covered with nodules of Te that are less than 100 nm in diameter (Fig. 2b). Figure 2c shows the CdTe/Te interface in cross-section and, evidently, the Te layer is fairly compact. A thin evaporated Au layer is observed to sit on top of the ~80 nm thick Te layer produced by the MAI treatment. For comparison, Figure 2d shows an SEM image of the CdTe/Au interface in a device processed without MAI treatment. Our previous work showed similar effects regardless of whether methylammonium bromide (MABr), chloride (MACl), or iodide was employed. However, the size of the islands is decreased in the order MAI > MABr > MACl [19]. Note that Te islands do not form when the sample is rinsed with IPA prior to the reaction step.

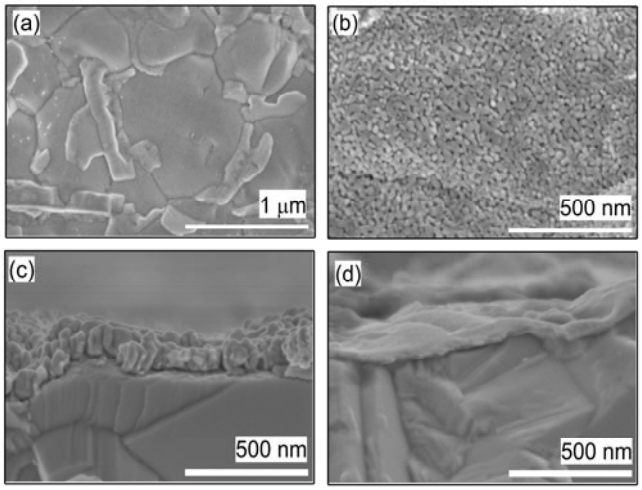

Fig. 2. SEM images of (a) $CdCl_2$ treated CdTe sample. (b) Surface morphology of a MAI treated sample using a 125 mM MAI solution and heated for 10 min at 125 °C. Cross-sectional SEM images of (c) MAI treated and (d) untreated CdTe devices with a Cu/Au back contact. Note that the Au layer is clearly visible in the untreated sample, but in the treated sample, Au is decorated on the Te layer.

C. Reaction Mechanism

MAI is one of the main precursors used in the fabrication of lead halide perovskite solar cells, and we recently showed that it readily forms $(CH_3NH_3)_2CdI_4$ (MA_2CdI_4) perovskite structures with Cd^{2+} ions [24, 25]. In those studies, MAI was mixed with $CdCl_2$ in an IPA solution, and MA_2CdI_4 perovskite spontaneously formed in solution at room temperature. In the present case, with no Cd ions initially present in solution, the MA salts evidently extract Cd from CdTe. Because the Te island formation only occurs after the sample is heated, we can propose the following reaction after the MAI film is formed:

$$MAI(s) + CdTe(s) \xrightarrow{\Delta} MA_2CdI_4(s) + Te(s) \qquad (1)$$

After reaction, the resultant MA_2CdI_4 perovskite can be rinsed in IPA due to its solubility [24, 25], leaving behind a Te layer on the CdTe film. The MAI treatment appears to be self-limiting since the surface morphology does not change significantly with changes in the MAI concentration. One reason could be that as the Te layer grows, it may form a layer that caps the CdTe, blocking further access of MAI to the CdTe surface. In addition to producing smaller Te islands, SEM and Raman spectroscopy analyses showed that the thickness of the Te layer was reduced in the order MAI > MABr > MACl. Since the processing was similar for each type of reaction, the data indicates that the formation energy of MA_2CdX_4 (where X is I, Br, or Cl) perovskites is reduced in the order Cl > Br > I [19].

It is clear that the MAI treatment selectively removes Cd from the CdTe surface through an interaction with the methyl ammonium cation. It is likely that any defective areas on the CdTe surface would have higher surface energy and therefore be more susceptible to Cd removal. This would suggest that Te layers created through the MAI treatment process should not only produce better electrical contact with the CdTe, but also produce a CdTe surface with fewer interface defects. As a result, better electrical properties at the back junction may be expected for devices with a Te layer formed using this method as compared to devices fabricated with an evaporated or sputtered Te layer.

D. Device Performances

To explore the effects of reaction temperature, at least 20 devices were made with 10 minute reactions at temperatures of 110, 125, 150, and 175 °C. Table I summarizes the photovoltaic performance parameters for the devices. A 3 nm thick layer of Cu, which is the optimum thickness for our standard device, was used.

TABLE I
DEVICE PARAMETERS FOR DIFFERENT REACTION TEMPERATURES

Temp	Voc (mV)	Jsc (mA/cm^2)	FF (%)	Eff (%)
Standard	796 ± 14	21.1 ± 0.2	74.6 ± 2.0	12.5 ± 0.4
Best	811	21.3	75.6	13.0
MAI treated sample heated at:				
110 °C	818 ± 5	21.2 ± 0.2	76.2 ± 0.8	13.2 ± 0.2
Best	821	21.7	76.7	13.7
125 °C	828 ± 3	21.2 ± 0.2	76.6 ± 1.3	13.5 ± 0.3
Best	830	21.5	77.5	13.8
150 °C	827 ± 3	21.2 ± 0.4	75.6 ± 1.2	13.3 ± 0.3
Best	826	21.7	75.7	13.5
175 °C	826 ± 4	21.1 ± 0.6	74.9 ± 1.2	13.0 ± 0.4
Best	833	21.4	75.8	13.5

For all treatment temperatures, the samples showed higher average V_{OC} values than the standard samples. FF improved with the treatment up to 125 °C, above which it began to decrease. The J_{SC} was not affected by the MAI treatment, indicating that the photocurrent generation in the CdS/CdTe devices is independent of the nature of the back junction and likely limited by the thick CdS layer that was used in these devices. Treatment at 125 °C resulted in the best performing devices with the highest average V_{OC}, FF, and PCE of 828 ± 3 mV, 76.6 ± 1.3%, and 13.5 ± 0.3%, respectively. The best device, with an efficiency of 13.8%, V_{OC} of 830 mV, J_{SC} of 21.5 mA/cm^2, and a FF of 77.5% was also obtained at the 125 °C reaction temperature. However, the difference in performance for the higher reaction temperatures was not significant. The V_{OC} and J_{SC} remained essentially constant, while a slight reduction in FF contributed to a small reduction in PCE.

The back contact of the devices reported in Table I were completed by depositing 3 nm of Cu and 40 nm of Au followed by a diffusion step at 150 °C. Because Cu_xTe is not formed at this temperature [10, 11, 13] (also, see Fig. 1), it is evident that Cu diffuses through the Te layer and into the CdTe [13]. Therefore, the back junction of our devices is likely to consist of a Cu-doped CdTe (CdTe:Cu) surface with a Te layer. Doping the CdTe surface by Cu to produce a p^+ region reduces the band bending at the back of the device and narrows the back barrier [7]. Since the amount of Cu in each of the devices in Table I is nominally the same, the interface between the CdTe and Te are expected to be quite similar in each case. Improvements in V_{OC} and FF for the treated devices can, therefore, be attributed to a lower back barrier and a reduced valance-band bending at the back contact as expected with the formation of a Te layer [14, 26]. The reduced FF for treatment temperatures above 125 °C remains unresolved but could be attributed to either additional etching at grain boundaries, which could decrease the shunt resistance, or to a slightly increased series resistance.

Table II shows the results from additional experiments designed to investigate the effect of the amount of Cu deposited on the MAI-treated CdTe back surface. The device stacks used for these experiments were treated with 125 mM MAI solution and heated for 10 min at 125 °C. The untreated devices prepared without Cu showed lower V_{OC} and FF values resulting in poor PCEs due to the high back contact barrier and band bending [3-7]. Dramatic improvements in the average V_{OC} and FF were observed with MAI treatment even when Cu was not used. As Cu was introduced we observed an improvement in all of the performance parameters for Cu thicknesses up to 2 nm. A 2 nm thickness showed the highest average V_{OC}, FF, and PCE values of 834 ± 2 mV, 77.2 ± 0.9%, and 13.8 ± 0.2%, respectively. The champion device, which exhibited an efficiency of 14.1%, Voc of 831 mV, J_{SC} of 21.8 mA/cm^2, and FF of 77.9%, was also achieved with 2 nm of Cu. For devices with more than 2 nm of Cu, the average V_{OC} decreased gradually, while the FF appeared to saturate near 77%. It is important to note that these results were achieved with a thick CdS layer. We note that with a current density of 26 mA/cm^2, which could be achieved with a thinner CdS layer, the PCE for the best device would be ~16.9%.

TABLE II

DEVICE PERFORMANCES FOR DIFFERENT AMOUNTS OF CU

Cu thickness	Voc (mV)	Jsc (mA/cm^2)	FF (%)	Eff (%)
Without MAI treated				
0 nm	649 ± 14	20.4 ± 0.3	68.4 ± 0.9	9.0 ± 0.3
Best	668	20.7	69.5	9.6
3 nm	796 ± 14	21.1 ± 0.2	74.6 ± 2.0	12.5 ± 0.4
Best	811	21.3	75.6	13.0
With MAI treated				
0 nm	775 ± 3	20.0 ± 0.1	70.7 ± 0.6	11.0 ± 0.1
Best	774	20.3	71.0	11.2
0.5 nm	817 ± 5	21.8 ± 0.1	75.3 ± 0.8	13.4 ± 0.2
Best	820	21.9	76.3	13.7
1 nm	821 ± 5	21.7 ± 0.1	74.9 ± 0.9	13.3 ± 0.2
Best	828	21.8	76.1	13.7
2 nm	834 ± 2	21.4 ± 0.2	77.2 ± 0.9	13.8 ± 0.2
Best	831	21.8	77.9	14.1
3 nm	828 ± 3	21.2 ± 0.2	76.6 ± 1.3	13.5 ± 0.3
Best	830	21.5	77.5	13.8
4 nm	821 ± 2	21.5 ± 0.1	76.6 ± 0.7	13.5 ± 0.2
Best	821	21.6	77.5	13.7
5 nm	814 ± 4	21.5 ± 0.2	76.5 ± 1.1	13.4 ± 0.2
Best	821	21.9	76.4	13.7
With evaporated Te				
3 nm	828 ± 6	21.4 ± 0.3	74.8 ± 1.6	13.3 ± 0.3
Best	839	21.8	75.6	13.8

Recently, Moore et al. showed that devices formed with an evaporated Te layer outperformed devices with a standard Cu/Au back contact [14]. To determine how our MAI-treated devices compare, we fabricated devices by evaporating 80 nm of Te followed by a Cu/Au back contact. The Cu thickness and diffusion time were varied to optimize the device performance. The best performing devices showed improved performance relative to the Cu/Au standard devices, but fell short of the performance of our best MAI treated device (See result in Table II).

The data suggest that the Te layer provides a low back barrier even in the absence of Cu. Thus, Cu may not be needed to produce a high degree of doping and a thin depletion region at the back surface. Following this line of thinking, then, the only role for Cu would be to increase the p-type doping level in the bulk. It is known that the degree of p-type doping of CdTe first decreases with increasing Cu concentration, then increases, and then again decreases [27]. When Cu is diffused through the Te layer and into the CdTe at moderate concentrations, it acts as an acceptor by substituting on Cd sites to produce acceptor doping [12]. Moderate amounts of Cu could increase the p-type carrier concentration and move the Fermi level toward the valence band, resulting in an increase in the open circuit potential of the device. At higher

Cu concentrations, however, the doping of CdTe is highly compensated by the formation of various defects and complexes [14]. The reduction in the amount of Cu needed for optimization of PCE relative to the standard device (2 nm versus 3 nm) is consistent with results found for devices prepared with elemental Te by evaporation [14]. The V_{OC} drop observed when the Cu thickness exceeded 2 nm may be attributed to a reduced p-type doping level due to compensation.

In addition to the improvements in V_{OC}, FF, and PCE that are available with MAI processing, it is interesting to note that MAI-treated samples, in general, lead to very high device-to-device reproducibility, indicating a wide, forgiving processing window.

E. Devices with Transparent Back Contact

With evidence for a low back contact barrier, we investigated the performance of devices formed with an ITO back electrode. In this case, the MAI treatment was followed by diffusion of 2 nm of Cu and the deposition of ITO by sputtering. Control samples without MAI treatment were also fabricated for comparison. Figure 3a presents the J-V curves and Table III shows the device performance for devices fabricated with and without MAI treatment.

TABLE III
THE J-V PARAMETERS FOR ITO BACK ELECTRODE

ITO with:	Voc (mV)	Jsc (mA/cm^2)	FF (%)	Eff (%)
Without MAI treated				
CdTe	471 ± 23	20.4 ± 0.4	51.3 ± 2.3	4.9 ± 0.3
Best	483	21.2	52.6	5.4
CdTe:Cu	810 ± 4	21.1 ± 0.4	57.2 ± 4.3	9.8 ± 0.7
Best	807	21.2	64.4	11.0
With MAI treated				
CdTe	748 ± 13	21.0 ± 0.4	57.9 ± 4.2	9.1 ± 0.8
Best	757	21.2	61.8	10.0
CdTe:Cu	820 ± 3	21.3 ± 0.2	66.3 ± 2.5	11.6 ± 0.5
Best	823	21.4	69.3	12.2

Without any MAI treatment and no Cu, the PCE was only ~5.0 %, with low V_{OC} and FF. With the introduction of 2 nm of Cu, V_{OC} and FF improved dramatically, resulting in a PCE of ~11.0% for the standard devices produced from this particular batch of TEC 12D/CdS/CdTe material. The MAI treatment, once again, produced significant improvements in V_{OC} and FF even without the use of Cu. When Cu was used, the Te layer further increased the V_{OC} and FF. As seen in previous experiments, the V_{OC} was higher for MAI-treated devices in comparison to Cu/Au devices, but the FF values were lower due to the high sheet resistance of the ITO. Our best device made with ITO back electrode had a PCE of 12.2% with V_{OC} of 823 mV, J_{SC} of 21.4 mA/cm^2, and FF of 69.3%. Figure 3b shows the transmission, reflection, and absorption spectra for device prepared with and without a Te layer by the MAI treatment. With a Te layer, the below gap optical transmission is ~40%. The present approach, without significant optimization, compares favorably to the results (PCE of 13.9%, ~50% below gap transmission) achieved with an ITO back electrode when a Cu_XTe layer was prepared by chemical etching followed by Cu evaporation and thermal processing [28].

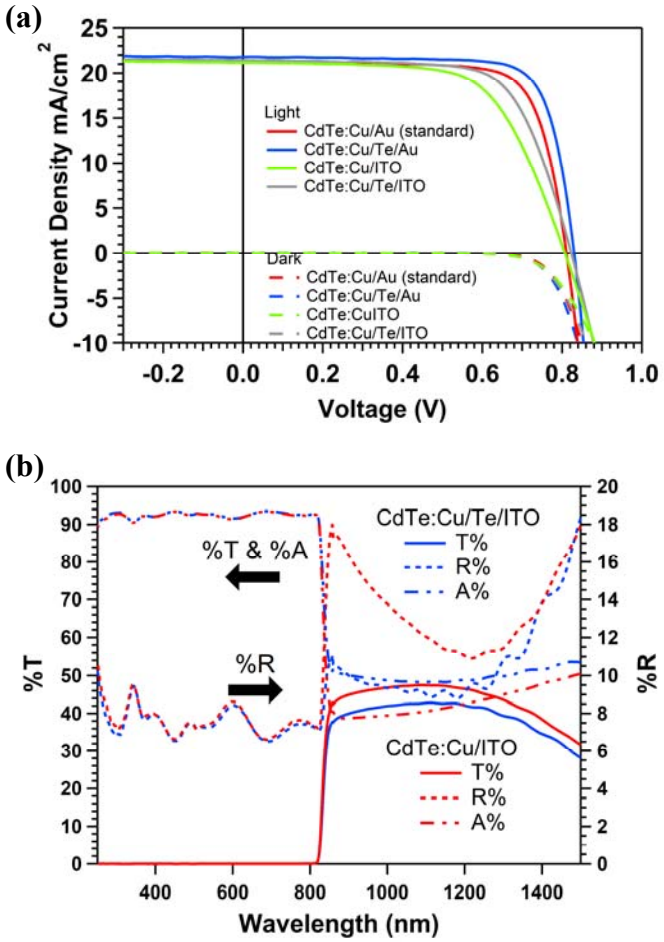

Fig. 3. (a) J-V characteristics of champion devices from the MAI treated and untreated CdS/CdTe samples with Au or ITO back electrodes. (b) Transmittance, absorbance, and reflectance of the MAI treated and untreated CdS/CdTe devices completed with the ITO back electrode.

F. Back Contact Barrier Heights

The temperature dependent dark J-V curves were analyzed to evaluate the effect of the MAI treatment on the energetic barrier to hole transport at the back contact of the device. J-V curves from 180 to 300 K and -0.5 V to +1.5 V were obtained for the various device configurations. Figure 4a shows the variation of the measured J-V curves with temperature for a standard Cu/Au device in forward bias, while Figure 4b shows the data for a Te/Cu/Au device that

was produced with the MAI treatment. Note that significantly higher forward bias currents are observed for the MAI-treated device for a given temperature and bias voltage, indicating a lower resistance back contact. The back contact barrier height, ϕ_b, can be extracted from an Arrhenius-type plot using the method presented by Niemegeers and Burgelman [29]. Figure 4c shows plots of ln (J/T^2) versus 1/KT for the devices.

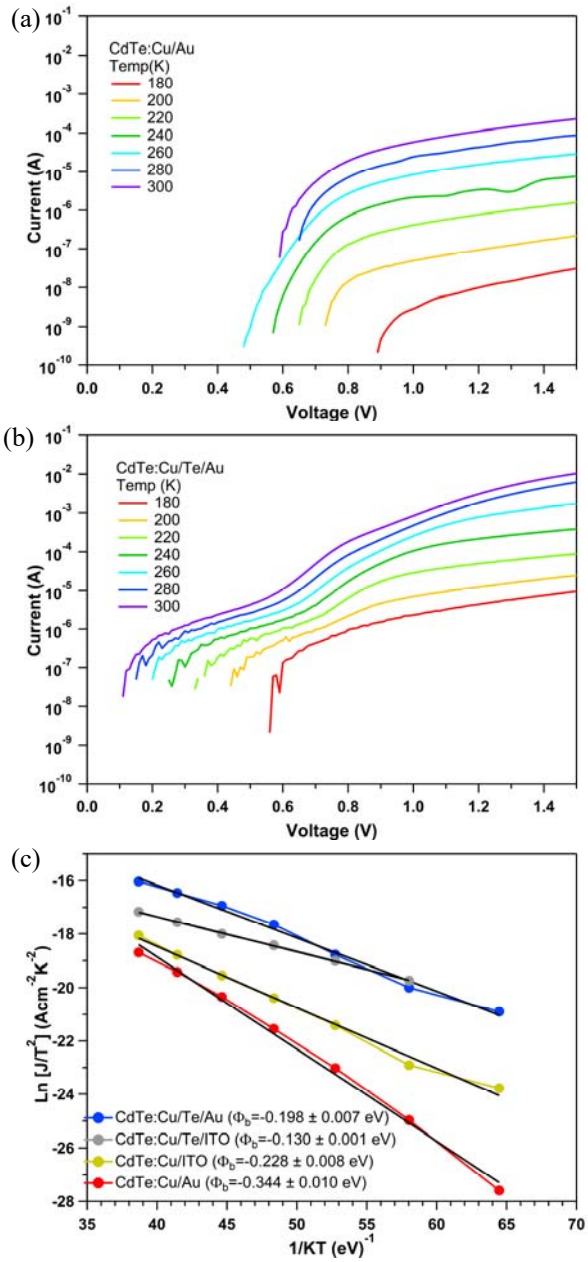

Fig. 4. Temperature dependence dark current-voltage (J-V) characteristics for (a) standard CdTe:Cu/Au and (b) CdTe:Cu/Te/Au devices. (c) Plots of ln (J/T^2) versus 1/kT at 1 V for CdTe:Cu/Au, CdTe:Cu/Te/Au, CdTe:Cu/ITO, and CdTe:Cu/Te/ITO devices.

Table IV shows the calculated ϕ_b values for the champion devices. The J-V curves for these devices under simulated AM 1.5G illumination (100 mW/cm^2) at room temperature can be seen in Figure 3.

TABLE IV
BACK CONTACT BARRIER HEIGHT FOR DEVICES MADE WITH AND WITHOUT TE PREPARED BY MAI TREATMENT

Device	ϕ_b (eV)
CdTe:Cu/Au	0.344 ± 0.010
CdTe:Cu/Te/Au	0.198 ± 0.007
CdTe:Cu/ITO	0.228 ± 0.008
CdTe:Cu/Te/ITO	0.130 ± 0.001

The barrier height of 344 meV for the CdTe:Cu/Au device is consistent with reported values [5, 30, 31]. When Te is introduced by the MAI treatment, the barrier was reduced by 146 meV. This barrier reduction should be accompanied by a similar reduction in band bending of the conduction band, which will reduce the amount of recombination at the back surface. Interestingly, for the untreated CdTe samples, Φ_b for the ITO back contact device was 116 meV lower than the standard Au electrode, indicating that the band alignment for ITO is better than that of Au. The ITO Φ_b was further reduced with the MAI treatment, yielding the lowest barrier of the devices measured at 130 meV, over 60% below the standard device configuration. This result suggests that with further optimization, the MAI treated CdTe devices with a transparent back contact may perform as well or better than CdTe:Cu/Te/Au devices. Furthermore, this reduced barrier and band banding should become more important for bifacial solar cells or when the CdTe thickness is reduced for window applications.

IV. CONCLUSION

We have shown that methylammonium iodide (MAI) can be simply and controllably reacted with CdTe surfaces to form a Te layer. MAI extracts Cd from the CdTe surface by forming the $(CH_3NH_3)_2CdI_4$ perovskite. SEM, XRD, and Raman spectra presented confirmed that thermal annealing is required for this reaction to occur. It was found that reacting a MAI thin film formed by spin-coating a 125 mM MAI solution with the CdTe surface at 125 °C for 10 min was the optimum MAI treatment. The optimized Cu thickness for the MAI-treated devices was reduced to 2 nm, as compared to 3 nm for the control devices.

The technique was successfully applied to increase the performance of CdS/CdTe devices with an ITO back electrode. The back barrier height was reduced with the MAI treatment for devices with Au and ITO back electrodes. High V_{OC} and FF values resulted in PCEs of 14.1% and 12.2% for the Au and ITO back contacts, respectively, for the MAI-treated

devices. In comparison, PCEs of 13.0% and 11.0% were measured for the Au and ITO electrode champion standard devices, respectively, which were prepared without the surface treatment. Devices prepared with the MAI treatment also outperformed devices fabricated with an evaporated Te layer.

V. Acknowledgement

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