Electronic Circuit Model for Evaluating S-Kink Distorted Current-Voltage Curves

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***Abstract* — So-called S-kink current vs. voltage (J-V) curves have been reported for solar cells based on numerous different materials and architectures, including but not limited to devices based on organic materials, chalcogenides including CIGS and CdTe, and passivated c-Si heterojunction devices. Reports frequently attribute the behavior to the presence of non-ideal energy offsets at one or both contacts. We report a method for modeling S-Kink behavior through the use of a modified diode circuit design for which an anti-parallel diode pair, in series with the main p-n heterojunction diode, serves to limit the current flow at voltage bias values near V_{OC}. The model provides a means to extract diode parameters from J-V plots exhibiting S-Kink behavior.**

***Index Terms* — s-kink distortion, circuit simulation, PSpice**

I. Introduction

Distortions to the current-voltage (J-V) curves of a photovoltaic device are typically caused by poor carrier transport at an interface/barrier. Large barriers at the back contact, such as the Schottky barrier known to exist for CdTe devices,[1, 2] will lead to a "roll-over" effect where the slope of the J-V curve is reduced at high forward bias. "S-Kink" behavior in J-V data has been previously observed in organic PV devices [3], CIGS (in the absence of blue photons)[4] and in c-Si HIT cells.[5]

The distinction between roll-over and the S-Kink shape is made clear in Fig. 1. Roll-over results when the main heterojunction diode is opposed by a diode resulting from, for example, a Schottky barrier at the back contact to a CdS/CdTe solar cell. As the device is brought into increasing forward bias, the back contact diode enters reverse bias for which device forward current is then limited. In contrast, an S-Kink J-V curve shows a reduction of current within the power producing quadrant, and a clear resumption of current in forward bias, a behavior distinctly different from roll-over. An electronic circuit model has been successfully developed for the roll-over J-V distortion[1] and applied to CdTe devices to extract the back contact barrier height[2] by means of a single diode in opposition to the main p-n heterojunction diode. To our knowledge, a similar model does not exist for evaluating S-Kink J-V curves. Here, we propose a circuit model to produce S-Kink J-V curves, and apply the model to simulate the S-Kink curves via SPICE software in OrCAD Capture CIS Lite.

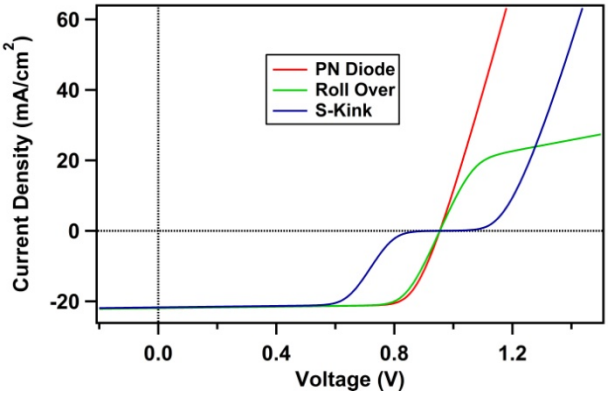

Fig. 1. Simulated J-V curves for the cases of a standard non-ideal p-n junction (red), roll-over (green), and S-Kink (blue).

II. S-Kink Distortion Model

We require a model which (1) allows current flow at low voltage bias, (2) restricts current flow near V_{OC}, and (3) allows current flow again at high bias ($V > V_{OC}$). Here, we start with the circuit model first proposed by Stollwerck and Sites[1] wherein the roll-over observed in CdTe devices is modeled using a two diode circuit model, where the back contact Schottky barrier is represented by a diode opposing the main junction diode. In the case of roll-over, current flow is restricted for voltages beyond V_{OC} due to the Schottky barrier entering reverse bias. In contrast to the case of roll-over, S-Kink J-V distortions indicate restricted current flow within an intermediate voltage range, and we therefore replace the back contact Schottky diode with an anti-parallel diode pair (i.e., a voltage clipper circuit), with shunt resistor R_{Shb}, as shown in Fig. 2.

The applied voltage is the sum of voltage drops across the three circuit segments circled in Fig. 2.

$$V = V_{main} + V_{back} + J * R_s \quad (1)$$

Under illumination at low bias ($V << V_{OC}$), the voltage clipper circuit element is pinned at a negative voltage. The main diode circuit elements, therefore, experience a voltage

drop higher than the applied bias. At reverse and low voltage, current flows freely through diode D_{b1}, while current is restricted through diode D_{b2}; the shape of the JV curve in this region is unaffected by the clipper circuit elements. As the applied bias increases, reverse bias restricts current flow through diode D_{b1}, initiating the S-Kink in the power-producing quadrant. As the voltage across the voltage clipper circuit, V_{back}, swings towards the positive limit (Fig. 3), current flows through the shunt resistor R_{Shb}, reducing the JV curve slope at V_{OC}. As current flow through diode D_{b2} turns on, voltage across the voltage clipper elements is pinned at the positive limit and current again flows with little resistance.

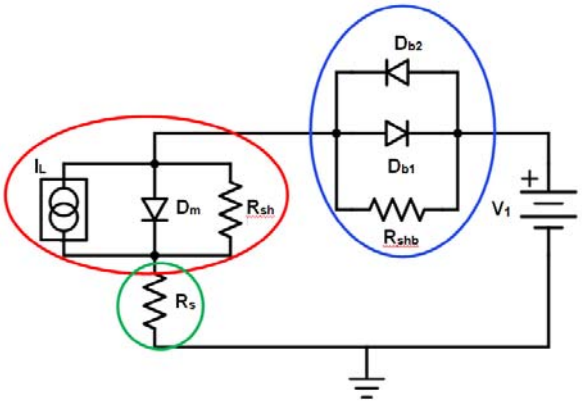

Fig. 2. Proposed circuit model for producing S-Kink J-V curves. Diodes D_{b1} and D_{b2} create the S-Kink while element R_{shb} influences the slope at V_{OC}. Colored circles coordinate with Fig. 3.

The main diode bias saturates at a voltage V_s and remains at that level until the applied bias reaches the value V_{S1}.

$$V_S = \frac{Ak_BT}{q}\ln\left(\frac{1}{J_{0,m}}\left(J_{SC}+J_{0,b1}+\frac{V_S}{R_{sh}}\right)\right) \quad (2)$$

$$V_{S1} = \frac{Ak_BT}{q}\ln\left(\frac{J_{SC}^2}{J_{0,m}*J_{0,b2}}\right) \quad (3)$$

, where A is the diode ideality factor. Under illumination the current through the main diode section is expressed as

$$J = J_{0,m}*\exp\left(qV_{main}/Ak_BT-1\right)-J_{SC}+\frac{V_{main}}{R_{sh}} \quad (4)$$

The current though the back contact is expressed as

$$J = -J_{0,b1}*\exp\left(qV_{back}/k_BT-1\right)+ J_{0,b2}*\exp\left(qV_{back}/k_BT-1\right)+\frac{V_{back}}{R_{shb}} \quad (5)$$

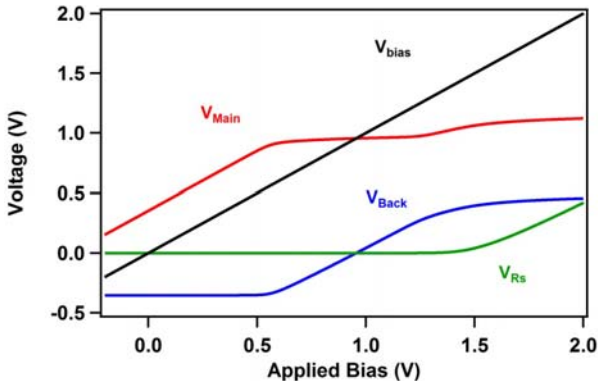

Fig. 3. Voltage drops across the main diode V_{main}, back diode pair V_{back}, and series resistor V_{RS} as a function of applied bias via SPICE simulations (trace colors coordinate with Fig. 2).

III. Simulation Discussion

We now explore the roles of the circuit elements on the resulting data. Fig. 4 depicts the influence of the reverse saturation currents $J_{0,b1}$ and $J_{0,b2}$ for the voltage clipper diodes. Diode D_{b1} controls the activation point of the S-Kink while D_{b2} controls the point at which current begins to flow again at higher forward bias. Should either of these reverse saturation currents $J_{0,b1}$ or $J_{0,b2}$ be too large, current flow is not restricted by the voltage clipper circuit and the S-Kink is not present (Fig. 4 red traces). As evident in Fig. 4, neither of the voltage clipper diodes (D_{b1} and D_{b2}) influence the V_{OC}, which is calculated by the standard equation

$$V_{OC} = \frac{Ak_BT}{q}\ln\left(\frac{J_{SC}}{J_{0,m}}+1\right) \quad (6)$$

, where $J_{0,m}$ is the reverse saturation current of the main diode, associated with the device's primary p-n junction.

As parameters $J_{0,b1}$ and $J_{0,b2}$ directly influence different sections of the S-Kink JV curve, we define here two points to be used in extracting the reverse saturation currents from experimental data. The S-Kink inflection point (at $V < V_{OC}$) is defined as V_A and extracted from the second derivative plots, as shown in Figure 5 for experimental data from a CdS/CdTe/FeS_2 NC/Au device at 200 K.[6, 7] Point V_B, at high forward bias, is defined here as the peak of the second derivative plot.

As shown in Fig. 6, SPICE simulations for various reverse saturation currents and short circuit currents reveal a linear dependence between the voltage offsets with V_{OC} and reverse saturations currents; ($V_{OC} - V_A$) versus $\ln(J_{0,b1})$ and ($V_B - V_{OC}$) versus $\ln(J_{0,b2})$.

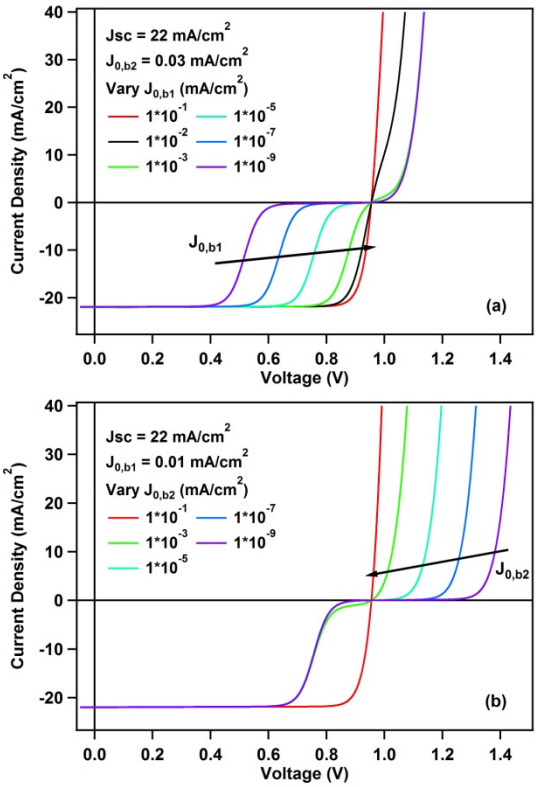

Fig. 4. S-Kink dependence on (a) $J_{0,b1}$ and (b) $J_{0,b2}$.

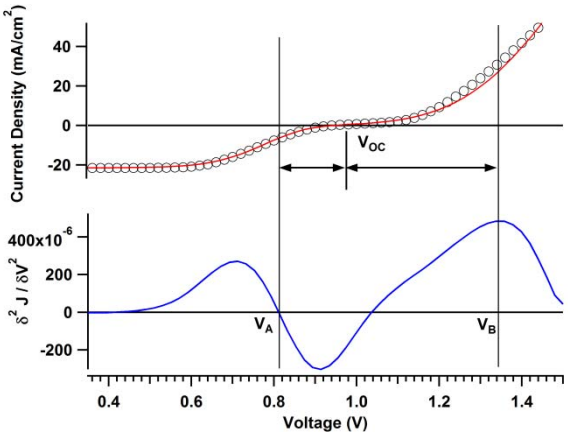

Fig. 5. Experimental S-Kink for CdS/CdTe/FeS_2/Au device (red) at 200 K, SPICE simulated data (black markers), and 2nd derivative plot identifying points V_A and V_B (blue trace).

Varying the short circuit current results in a discrete shift of the traces in Fig. 6. Furthermore, one must consider the influence of parasitic resistances on the position V_A and V_B; particularly series resistance which alters the slope at high forward bias and reduces fill factor. Our simulations indicate a linear dependence of V_A on short circuit current and parasitic resistances.

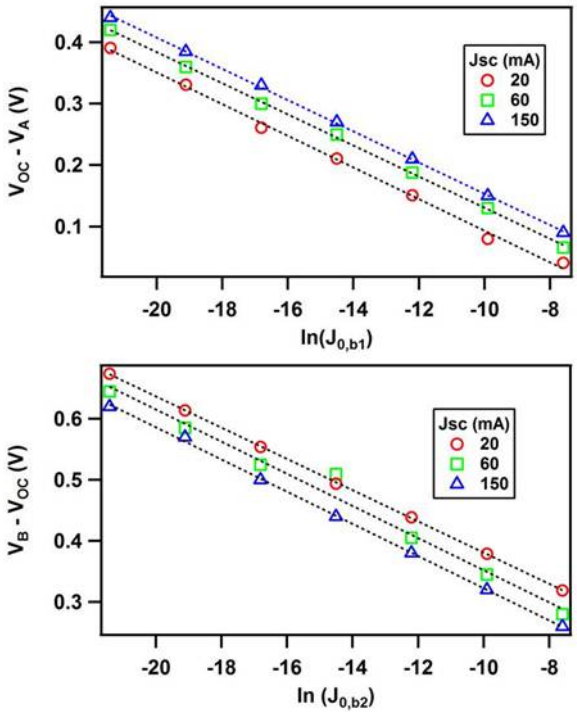

Fig. 6. Influence of J_{SC} on S-Kink voltage offsets ($V_{OC} - V_A$) (top) and ($V_B - V_{OC}$) (bottom).

From these simulation results we devise the following equation to extract $J_{0,b1}$ from experimental data.

$$J_{0,b1} = \frac{J_{SC}}{\exp\left(q\left(V_{OC} - V_A - \frac{J_{SC}}{2} * \left(\frac{R_S * R_{Sh}}{R_S + R_{Sh}}\right)\right) \Big/ k_B T\right) - 1} \tag{7}$$

, where R_{sh} is the shunt resistance evaluated at J_{SC}. However, the influence of series resistance on $J_{0,b2}$ exhibits a non-linear dependence inconsistent with any simple mathematical relation. Additionally, there is a strong influence of R_{Shb} and $J_{0,b2}$ on point V_B when series resistance is large ($R_S > 5\ \Omega\ cm^2$). A simplified equation for $J_{0,b2}$ incorporating these dependencies has not been found and so, for now, we omit the parasitic resistance influence on V_B.

$$J_{0,b2} = \frac{1}{J_{SC} * \left[\exp\left(q\left(V_B - V_{OC}\right) \Big/ k_B T\right) - 1\right]} \tag{8}$$

Finally, we provide an approach for predicting the net current flow given initial guesses for circuit parameters. Predicting the voltage drop across the back diode elements, V_{back}, via the piecewise function in Equation (9), one may then predict the net current flow via Equations (1) and (2),

allowing the user to visually evaluate the residual as parameters are varied.

$$V_{back} = \begin{cases} \frac{k_B T}{q} \ln\left(\frac{-J_{0,b1}}{J - V_{back}/R_{shb}} \right) & ,V < V_1 \\ V - \frac{k_B T}{q} \ln\left(\frac{J_{SC}}{J_{0,m}} \right) & ,V_1 < V < V_2 \\ \frac{k_B T}{q} \ln\left(\frac{J - V_{back}/R_{shb}}{J_{0,b2}} \right) & ,V_2 < V \end{cases} \quad (9)$$

, where V_1 and V_2 are defined as a point midway between V_{OC} and the points V_A and V_B identified from the second derivative plot, Figure 5, $V_1 = (V_A + V_{OC})/2$ and $V_2 = (V_B + V_{OC})/2$.

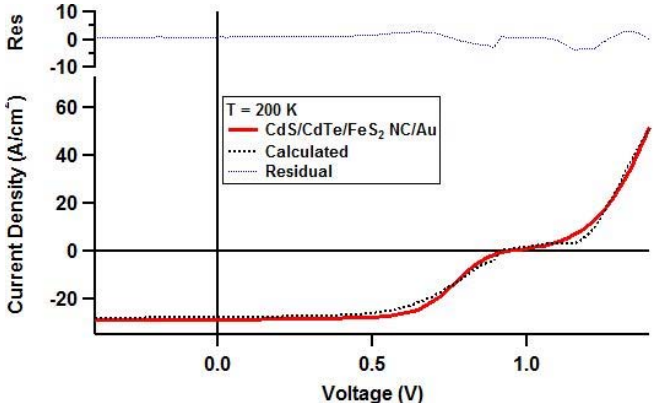

Fig. 7. Comparison of predicted JV curve via manually guessed circuit parameters with experimental data at 200 K for the CdS/CdTe/FeS_2 NC/Au device.

IV. Conclusions

A circuit model, representing the back contact with an anti-parallel diode pair, has been demonstrated to reproduce S-Kink JV plots via SPICE simulations. The influence of various circuit element parameters have been predicted via SPICE simulations in order to develop equations for estimating circuit element values from experimentally obtained data. A comparison between predicted JV curves and experimental data has also been provided. Further extension of the S-Kink current voltage model requires a more reliable identification of reverse saturation current $J_{0,b2}$ which corrects for the non-linear influence of parasitic resistances on $J_{0,b2}$ via Equation (8). In addition, the utility of the model in enabling insights into the materials science will require correlation of the model's diode characteristic parameters with the device's physical parameters which determine current flow.

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