Effects of electric field on thermal and tunneling carrier escape in InAs/GaAs quantum dot solar cells

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ABSTRACT

The effects of electric field on carrier escape in InAs/GaAs quantum dots embedded in a *p-i-n* solar cell structures have been studied by quantum efficiency. Via band structure simulation, effective barrier height of carriers inside QDs is reduced with increasing local electric field, so tunneling and thermal escape are enhanced. At 300K, when electric field intensity is below 40kV/cm, thermal escape is dominant in all confined states in QDs; when electric field intensity is above 40kV/cm, tunneling is dominant in shallow confined states and thermal escape is dominant in the ground state of QDs.

Keywords: electric field, InAs/GaAs quantum dots, photovoltaic cells, carrier escape

1. INTRODUCTION

Recent progress in self-assembled InAs/GaAs quantum dots (QDs) has promoted the developments of bandgap engineering [1] for application in a multijunction solar cell [2] and the intermediate band solar cells (IBSCs) [3][4] [5]. Due to the quantum size effect, the absorption and emission energy can be tuned by changing the size of InAs/GaAs QDs, which leads to enhanced sub-GaAs-bandgap absorption. However, the collection of carriers from the QDs is essential to improve the energy conversion of QDs embedded solar cells, which depends on the carrier escape process. There are generally three ways to enable photo-excited carrier escape from QDs, including thermal activation, tunneling and optical two-photon sequential absorption. No restrictions are placed among these escape mechanisms for applications of bandgap engineering, but tunneling and thermal escape compete with the sequential absorption process, thus reduction of tunneling and thermal escape is critical for the realization of IBSCs [6].

Since in many applications, InAs QDs are usually embedded in the intrinsic region of a pin GaAs solar cell, to better understand device physics and improve carrier collection, it is important to investigate the effect of the electric field on carrier escape. To date, the electric field effects on the carrier dynamics in InAs/GaAs QDs have been investigated via a combination of photocurrent [7] and photoluminescence [8] or by differential transmission spectroscopy[9]. The authors in these studies demonstrated that thermal activation and tunneling is dominant in carrier escape from QDs. They also showed that the rate of carrier escape increases with increasing the intensity of the electric field.

In this work, the effect of electric field strength on the effective barrier height and related tunneling rate and thermal escape rate were estimated from the band structure simulation. Voltage bias dependent external quantum efficiency (EQE) measurements at room temperature were used to detect the enhanced tunneling and thermal escape rates with increasing field. Temperature dependent EQE measurements were then used to distinguish the importance of thermal activation in carrier escape under varied intensity of electric field. It is found that both tunneling and thermal escape are enhanced with increased local intensity of electric field. Although thermal escape is dominant in the ground state escape, tunneling becomes dominant in the shallow confinement above 40kV/cm.

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2. Sample set and Experiment

This work provides an extension of the work by Driscoll *et al* .[10], which showed the combined effects of the QDs position and bulk doping profile on the performance of *pin*-GaAs solar cells. Similar to Driscoll *at al.*, three QD embedded *pin* GaAs solar cells with varied QD placement were investigated. The structures were grown using a low-pressure rotating disk metal organic vapor phase epitaxy (MOVPE) reactor (Veeco P125LDM). Growth temperature was monitored in-situ using an emissivity corrected optical pyrometer. All samples were grown on 350 µm thick Si doped GaAs (100) substrates misoriented toward the (110) direction. The misorientation angle was 2º.

As can be seen in Figure 1 a five-layer superlattice of QD was inserted into the 600 nm intrinsic region of a *pin* GaAs solar cell at the center (centered QDSC), 33 nm from the p-type emitter (emitter shifted QDSC), or 33 nm from the n-type base (base shifted QDSC) [10]. The superlattice (periodicity 12 nm) consisted of repeating InAs QDs, GaP strain compensation, and GaAs spacer layers. The QDs were grown at 500ºC with InAs coverage of 1.8 monolayers (ML). After growth of a low temperature GaAs capping layer, temperature was ramped to 585ºC for growth of the GaAs spacer layers and a 1.15 nm thick GaP strain compensation layer. Then the total thickness of intrinsic region was fixed at 600 nm by capping with unintentionally doped GaAs. The average hemisphere-shaped QDs size is 2-3 nm in height and 20-25 nm in diameter [11]. For the solar cell, thin (50 nm) InGaP front and back surface layers are employed to reduce surface and interface recombination. The emitter consisted of 500 nm of Zn-doped GaAs with a doping density of 2×10^{18} cm^{-3} and the base consisted of 2000 nm Si-doped GaAs with a doping density of 1×10^{17} cm^{-3}. Finally, a heavily doped GaAs layer is used to facilitate Ohmic contact formation. Solar cells were fabricated using standard III–V processing and microlithography techniques. Ohmic contacts to a thickness of 1 µm were made to the p- and n-type regions using thermally evaporated Au/Zn/Au and Au/Ge/Ni/Au metallization, respectively. Individual cells were isolated using wet chemical etching techniques. Anti-reflective coatings were not used in order to focus on the QD incorporation. EQE measurements were performed on 1×1 cm^2 pads without grid finger.

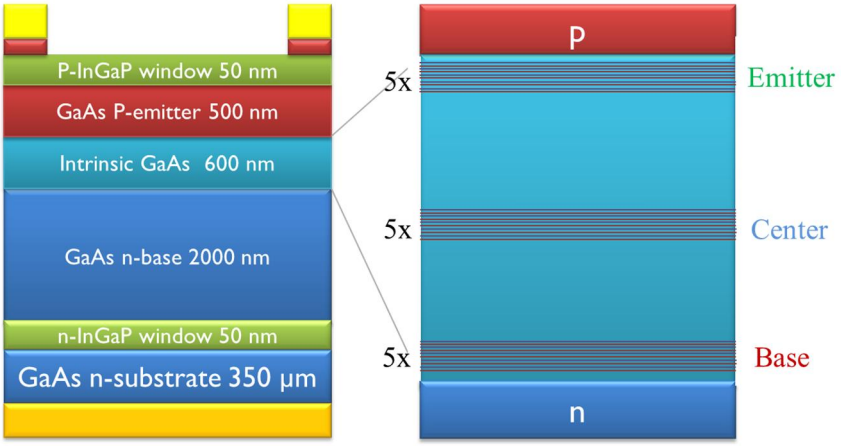

Figure 1. Structural layer layout for QD embedded GaAs p-i-n solar cell device

Room temperature quantum efficiency measurements were taken with a Newport IQE-200 Spectroradiometric Measurement system and voltage bias was applied with a Stanford 570 low-noise current preamplifier and a Stanford Research Systems SR830 DSP lock-in amplifier. Temperature dependent EQE and low temperature voltage bias EQE were completed with OL750 Spectroradiometric Measurement system. The measured QDSCs were cooled by a Cryoindustries 10K M-22 cryo-system.

3. Theoretical Approach

In order to theoretically investigate the effect of electric field, band structure of InAs/GaAs quantum dots embedded in the intrinsic region of a p-i-n solar cell were simulated based on a finite-difference discretization of the 8-band ***k·p*** Hamiltonian [12] for the three investigated samples. The programming code for the simulation is similar to the Nextnano3 software [13]. Height, average diameter of single quantum dot, and wetting layer thickness were set at 3 nm, 16 nm, and 0.5 nm,

respectively. In addition, 1.3 nm GaP as strain compensation layer was inserted between the dots, so the total dot-dot distance was set at 14 nm. All simulations were done using a temperature of 300K.

Figure 2(a), 2(b), 2(c) show the simulation results at 300K of the band structures of base shifted, centered, and emitter shifted QDSC, respectively. Because of non-negligible n-type background doping in the intrinsic region, the intensity of electric field increases from 5 kV/cm near the n-type base to 50 kV/cm near the p-type emitter [10]. The band bending experienced by the QDs at the three positions is illustrated, which is due the electric field variation with depth across the 600 nm intrinsic region. As can be seen, five quantum dots and related barrier layer are shown in the simulation results under zero bias. Two localized energy states of electrons can be seen in each QD. Because of the heavier effective mass of the hole than electron [13], there are too many bound states of holes to be shown, however the escape process we have focused on in this work is from the two bound electron states.

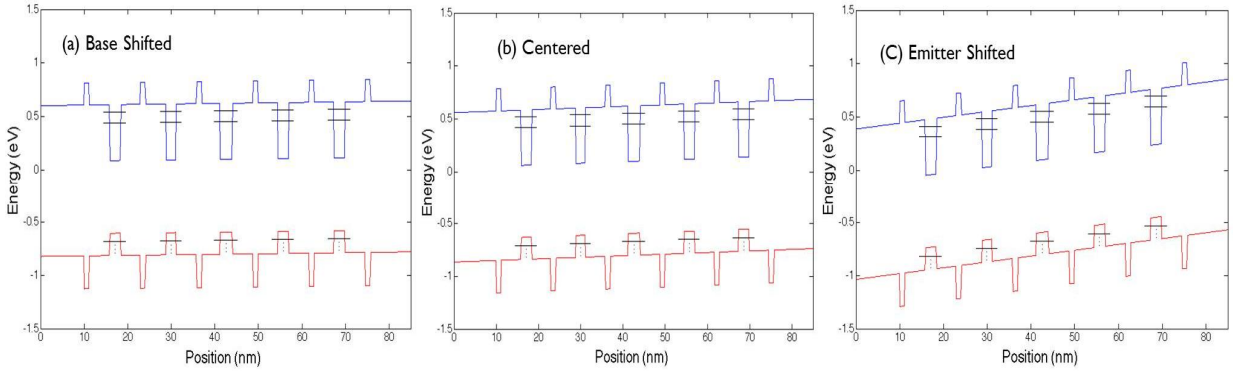

Figure 2. Calculated band structure of different QD placement: (a) Base shifted, (b) centered, and (c) Emitter Shifted.

The average barrier heights for ground state electrons extracted from Figure 2 is 168 meV (base-shifted QDSC), 167 meV (centered QDSC), 159 meV (emitter-shifted QDSC), while that of the excited state are 68 meV (base-shifted QDSC), 64 meV (centered QDSC), 60 meV (emitter shifted QDSC). Here the average barrier height refers to the energy difference between a confined energy state and conduction band edge of the third layer of QD. Because of increasing electric field [10], compared to the base shifted QDSC, the average barrier height of the ground state and the excited electrons both slightly decrease (around 9 meV) in the emitter shifted QDSCs.

Making use of the extracted barrier height and band structure profile from Figure 2, the tunneling time and thermal escape time can be estimated. The thermal assisted escape time τ_{th} and approximate tunneling time τ_{tun} for different energy level are given by the equations below [14] [15]:

$$\frac{1}{\tau_{th}} = \frac{1}{L_z}\sqrt{\frac{kT}{2\pi m_Q}}\exp\left(-\frac{\Delta E_h}{kT}\right) \qquad (1)$$

$$\frac{1}{\tau_{tun}} = \frac{1}{L_z^2}\frac{n\pi\hbar}{2m_Q}\exp\left(-\frac{2}{\hbar}\int_0^b \sqrt{2m_b(qV(z) - E_n - qFz)}\,dz\right) \qquad (2)$$

where m_Q is the carrier's effective mass in the quantum confinement (m_Q=0.06m_0 [16]), m_b is the carrier effective mass in the barrier, L_z is the width of the confining structure and ΔE_h is the barrier height, b is barrier thickness, $V(z)$ is arbitrary potential between 0~ΔE_h due to variations in band edges in epitaxial layers close to the dots, k is Boltzmann constant and T is temperature. As can be seen in Figure 3, first, thermal escape is dominant for the ground state electron escape from QDs in all three QDSCs at 300K. Tunneling time in ground state is only practical (3.6 ms), albeit very slow compared to thermal escape, in the emitter shifted QDSC. For the excited states, thermal escape is still dominant at zero bias. Nevertheless, with increasing field intensity, the difference between tunneling time and thermal escape time is reduced from an order of 10^7 to 10^1. From equation (1) and (2), the tunneling is dominant for electron escape from excited states inside QD if the intensity of electric field is above 50 kV/cm. With increasing the intensity of the built-in electric field from base-shifted QDSC to emitter shifted QDSC, thermal escape time of electrons slightly decrease, while tunneling time decreases exponentially.

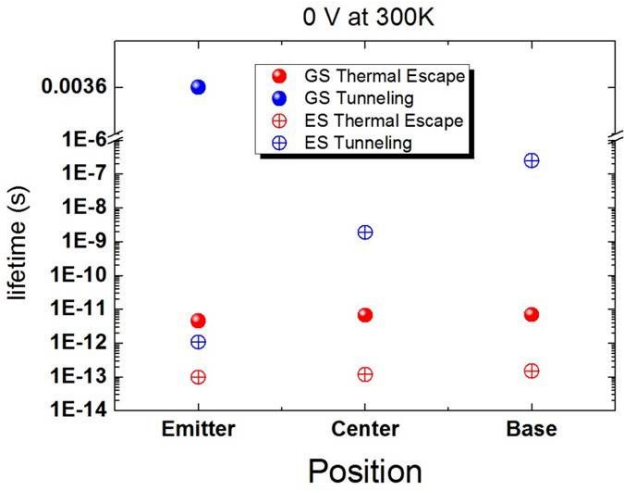

Figure 3 Lifetime of the tunneling and thermal escape in the three investigated QDSCs.

4. Results and Discussion

To detect the effect of electric field on carrier collection at room temperature, Figure 4(a) shows the 300K EQE. Five peaks in total including EQE from wetting layer (WL, 920 nm), the excited states (920 nm to 1020 nm), and the ground state (GS, 1050 nm) can be observed. Due to the slightly n-type back ground doping, the intensity of the built-in electric field increases towards the emitter. Because of local field enhanced tunneling and thermal escape, EQE from the emitter shifted is highest, which is well correlated with the rate calculation in Figure 3.

Figure 4(b) shows the EQE as a function of reverse bias from the WL. EQE from the three QDSCs increase with reverse bias voltage, which is due to electric field enhanced tunneling and thermal escape, because the intensity of electric field increases with reverse bias. Furthermore, the centered QDSC shows the most sensitivity to the change of electric field among the three cells. With increasing reverse bias from 0 to -4 V bias, center QDSC shows ~7% (relative) per volt increase in EQE, while the base and emitter increase 5% (relative) per volts and 2% (relative) per volts, respectively. This indicates a non-uniform change in the intensity of electric field with bias voltage across i-region, due to slight background doping of the i-region.

Figure 4(c) shows the EQE vs bias from the ground state of QD. EQE of both base and centered QDSCs increases with increasing reverse bias, while EQE in emitter QDSC is stable with reverse bias voltage. This indicates that the carrier in the ground state of emitter-shifted QDSC are already efficiently collected at zero bias, due the enhanced tunneling and thermal escape in a high electric field. Additionally, because thermal escape is dominant in the carrier escape from the ground state, the change with bias is less pronounced in the ground state than that in the WL.

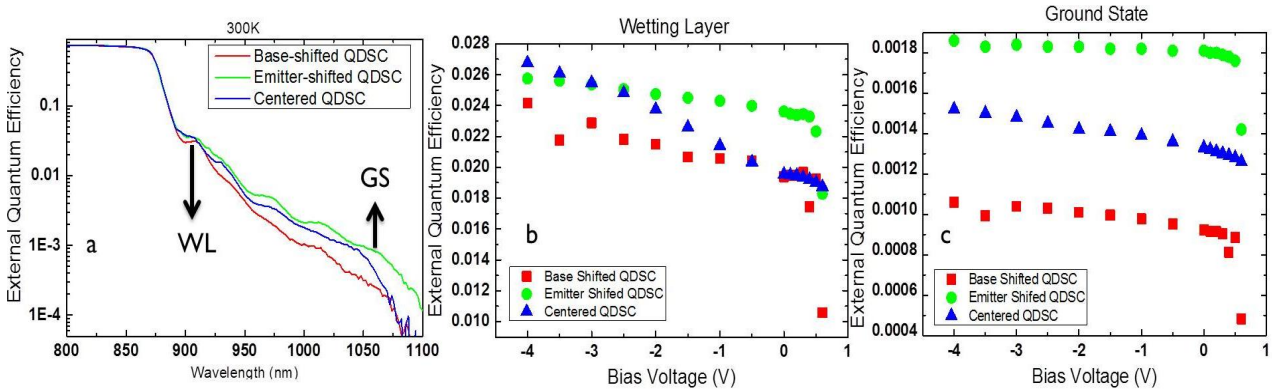

Figure 4 (a) Room temperature EQE, room temperature bias dependent EQE in (b) Wetting layer (c) Ground state.

To further confirm the predictions as outlined above, Figure 5(a) shows the temperature dependent EQE in the wetting layer (920 nm at 300 K). As can be seen, with decreasing temperature, the value of EQE from the shallow confinement (WL) in emitter shifted sample decrease least in the three QDSCs. At low temperatures, carrier escape from the emitter and center QD samples is possible due to carrier tunneling. The value of EQE in base-shifted sample decrease towards to zero around 50K, because thermal activation is dominant in all confined states under low electric filed intensity. Figure 5(b) shows the temperature dependent EQE in the ground state (1050 nm at 300K). As shown previously, thermal escape will dominate the ground state, thus when temperature is below 50K, the EQE from the ground state is reduced towards zero in all QDSC. This phenomenon is consistence with the calculation shown in Figure 3.

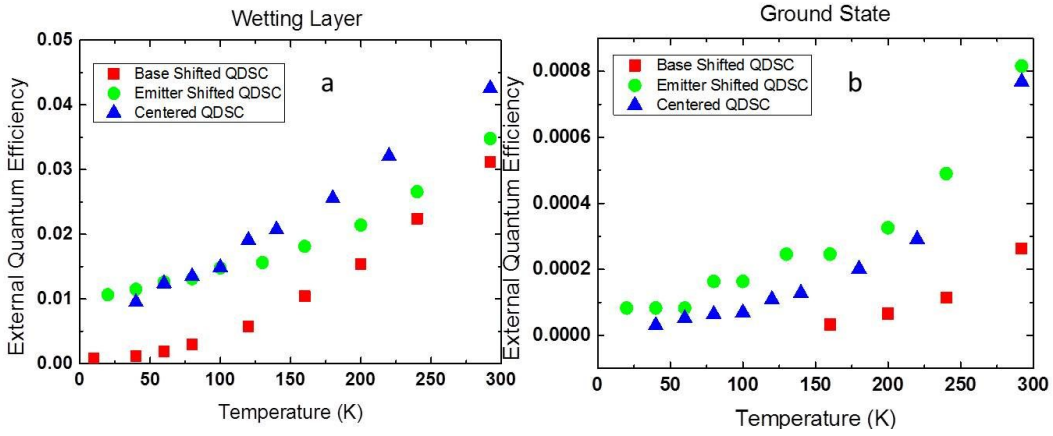

Figure 5 Temperature dependent EQE from (a) Wetting layer and (b) Ground state.

5. Conclusion

Due to background doping, the local electric field in the intrinsic-region decreases from near the p-emitter to near n-base for an InAs QDSC. Thermionic emission and carrier tunneling are shown as primary means of carrier collection. Local electric field enhances carrier tunneling and thermal escape inside InAs/GaAs QDs. With local field intensity increasing, tunneling becomes dominant in the shallow confinement; while thermal escape is dominant in deep confinement. Due to highest electric field intensity in emitter sample, most carriers can be collected at zero bias and EQE from the emitter shifted QD is the most stable with bias voltage and temperature.

ACKNOWLEDGEMENTS

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