ACS APPLIED MATERIALS & INTERFACES

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Research Article

Reduced Recombination and Improved Performance of CdSe/CdTe Solar Cells due to Cu Migration Induced by Light Soaking

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Cite This: https://doi.org/10.1021/acsami.1c23937

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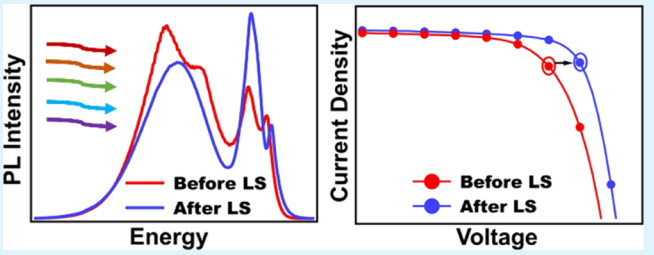
ABSTRACT: The performance of CdTe solar cells has advanced impressively in recent years with the incorporation of Se. Instabilities associated with light soaking and copper reorganization have been extensively examined for the previous generation of CdS/CdTe solar cells, but instabilities in Cu-doped Se-alloyed CdTe devices remain relatively unexplored. In this work, we fabricated a range of CdSe/CdTe solar cells by sputtering CdSe layers with thicknesses of 100, 120, 150, 180, and 200 nm on transparent oxide-coated glass and then depositing CdTe by close-spaced sublimation. After $CdCl_2$ annealing, Cu-doping, and back metal deposition, a variety of analyses were performed both before and after light soaking to understand the changes in device performance. The device efficiency was degraded with light soaking in most cases, but devices fabricated with a CdSe layer thickness of 120 nm showed reasonably good efficiency initially (13.5%) and a dramatic improvement with light soaking (16.5%). The efficiency improvement is examined within the context of Cu ion reorganization that is well known for CdS/CdTe devices. Low-temperature photoluminescence data and V_{oc} versus temperature measurements indicate a reduction in nonradiative recombination due to the passivation of defects and defect complexes in the graded $CdSe_xTe_{1-x}$ layer.



KEYWORDS: *$CdSe_xTe_{1-x}$, light soaking, bias soaking, Cu migration, front interface*

INTRODUCTION

Cadmium telluride-based photovoltaic (PV) devices have demonstrated excellent performance and durability with a record efficiency of 22.1% for laboratory scale devices[1] and more than 30 GW_P of modules shipped.[2] Recent performance increases have been enabled by the introduction of Se to create band gap grading[3−5] at the front of the device. CdSe alloys with CdTe during growth and subsequent chloride treatment to produce a graded $CdSe_xTe_{1-x}$ (CST) layer that may have a band gap as low as 1.38 eV due to band gap bowing.[6] The enhanced blue and red responses in CST/CdTe devices as compared to the traditional CdS/CdTe structure are attributed to, respectively, the improved photoactivity in the portion of the CST layer, which is in the zincblende phase ($x < 0.4$), and the associated band gap lowering.[7] In addition to enhancing the current, Se alloying also results in better band alignment and reduced recombination rates near the front interface, as well as longer minority carrier lifetimes.[5,8,9]

When a CdSe layer is used at the front of the device to provide a Se source for forming the CST layer, the initial CdSe thickness is critical. Near-complete consumption of the layer during processing is essential to avoid a residual unreacted wurtzite-phase CdSe layer which would be photoinactive and lower the blue response.[4,5,7] Poplawsky et al.[4] found that a 50 nm thick CdSe was too thin to improve the device performance, while a 100 nm layer produced the desired Se alloying and good junction characteristics. Thicker buffer layers left residual CdSe that reduced the short-circuit current (J_{sc}).[4,10] Though the extent of Se diffusion and subsequent thinning of the CdSe layer is likely dependent on the deposition conditions for the CdTe film, a recent study has suggested that the primary driver of Se diffusion is the $CdCl_2$ treatment.[11]

Copper has played a critical and complicated role in traditional CdS/CdTe PV technology. When Cu is present at an optimum level, the carrier concentration is increased, defects are passivated, and the photoconversion efficiency is

Received: December 10, 2021
Accepted: April 7, 2022

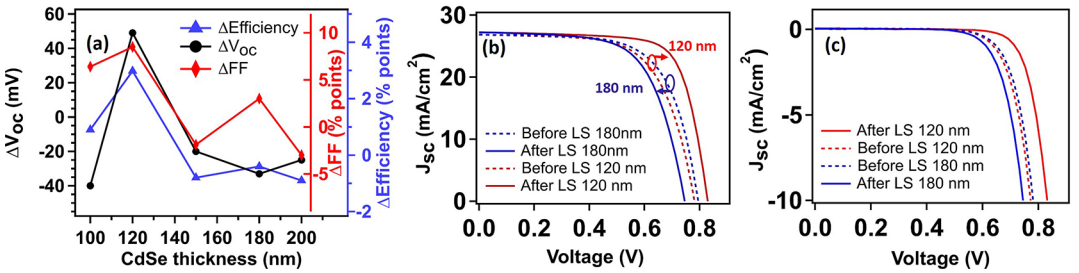


Figure 1. (a) Changes (Δ) in absolute PV parameters (V_{oc}, FF, efficiency) after LS under open-circuit condition at 35 °C for 16 h for devices with different starting CdSe thicknesses, (b) $J-V$ curves before and after the LS for devices with CdSe thicknesses of 120 and 180 nm measured under light illumination and (c) in the dark.

improved.[12,13] Cu is also used to manage the barrier height of the back electrical contact.[14] Copper redistribution is known to lead to device degradation, particularly when the device is operated at voltages less than the maximum power point (MPP) and at elevated temperatures.[14−16] The degradation can be manifested in several ways—as a drop in V_{oc}, the development of roll-over in the current density−voltage ($J-V$) curve, increased series resistance, drop in shunt resistance, or general contact degradation.[15,17−20] Resting in the dark for a period of time can lead to partial recovery of the performance.[21,22] These observations are collectively explained in terms of the mobility of Cu^+ ions and the Cu reorganization that occurs when the concentration or electric field gradients within the device are changed.[15,20]

Copper reorganization also plays a role in device "wake-up" in traditional CdS/CdTe devices. Guo et al. light soaked samples at short-circuit at 60 °C and observed degraded performance.[23] However, when the light soaking (LS) was done under open-circuited conditions or when a forward bias was applied to the device in the dark, an improvement was seen. The changes in performance were modeled using a simplified dopant compensation picture that considered coupled equilibria between Cu_{Cd}^{-} acceptors, neutral Cu_{Cd}^{0} species, and the reorganization of Cu_i^+ donors.[23] Copper reorganization will also alter the population, degree of association/dissociation, charge, and spatial distribution of related defect complexes that form from the possible individual point defects, including those associated with chlorine.[24] A variety of complexes with energy levels near the valence band maximum have been identified,[24] and changes in the recombination rates associated with these and other point defects in the depletion region can place the device in an improved operational state that is stable over a time scale longer than daily variations so long as shallow traps are not involved.[22]

While there is an extensive knowledge base on Cu movement and related stability issues in traditional CdS/CdTe devices, there is a comparative lack of information on the topic for CST/CdTe devices. Recent experimental evidence suggests that copper doping is significantly altered due to the presence of a Se gradient.[12] The Se concentration in the front of the device varies significantly over a distance of ∼0.5−1 μm,[25,26] and it may be expected that the defects and their interactions with both Cl and Cu will be different from those encountered in CdS/CdTe where the ternary region is significantly thinner. In fact, recent simulations indicate that the defect equilibria and related formation energies, ionization levels, and reaction barriers are all functions of the Se concentration in the CST layer.[27]

In this contribution, we examine the impact of LS on the performance of devices that were fabricated with different CST layers and doped with Cu. Initial CdSe layers ranging in thickness from 100 to 200 nm were deposited on transparent oxide-coated glass by sputtering, and CdTe was subsequently deposited by close-spaced sublimation (CSS). The deposited stacks were $CdCl_2$ treated, doped using $CuCl_2$, and finished into devices. Related details are provided in the Materials and Methods section. The $J-V$ parameters were measured before and after LS. After LS, an increase in V_{oc} was found for only one specific CdSe layer thickness (120 nm). LS also increased the activation energy for carrier recombination in this case, as measured by V_{oc} versus temperature measurements, and room temperature and low-temperature photoluminescence (PL) spectroscopy confirmed that the performance enhancement was due to a reduction in recombination near the front interface. The mechanism for the improvement is discussed within the context of copper migration.

RESULTS AND DISCUSSION

Figure 1a shows the changes in the key PV parameters for devices fabricated with varied CdSe thicknesses (100, 120, 150, 180, and 200 nm) and light-soaked for 16 h under open-circuit condition (1 sun at 35 °C). The stacks were deposited, $CdCl_2$ treated, and doped with Cu as described in the Materials and Methods section. The light-soak time of 16 h was chosen because the device performances were fairly stabilized after this time. Three out of five of the thicknesses (100, 120, and 180 nm) showed an improvement in fill factor (FF), while only the 120 nm device showed an improvement in V_{oc}. The J_{sc} was improved in only the 100 and 120 nm devices. The combined changes in V_{oc}, FF, and J_{sc} led to improved efficiencies for only the 100 and 120 nm CdSe devices. The improvement in efficiency for the 100 nm CdSe device was relatively small, from a low base value (e.g., from 9.5 to 10.5%), while the change in efficiency for the 120 nm CdSe device was significantly larger and from a larger base (from 13.5 to 16.5%). Clearly, small changes in CdSe thickness can lead to substantial changes in the device performance with LS. The device parameters relating to Figure 1a are presented in Figure S1. The data shown in Figure 1a are for the highest efficiency device of each type, but the same trends were observed for populations of ∼30 cells for each group (Figure S2).

Figure 1b shows the light $J-V$ curves before and after LS for representative devices constructed with 120 and 180 nm CdSe layers, while Figure 1c shows the dark $J-V$ data for the same devices. The 120 nm device shows improvement in the diode turn-on voltage after light-soak in both cases, suggesting a reduction in the concentration of active defects in the

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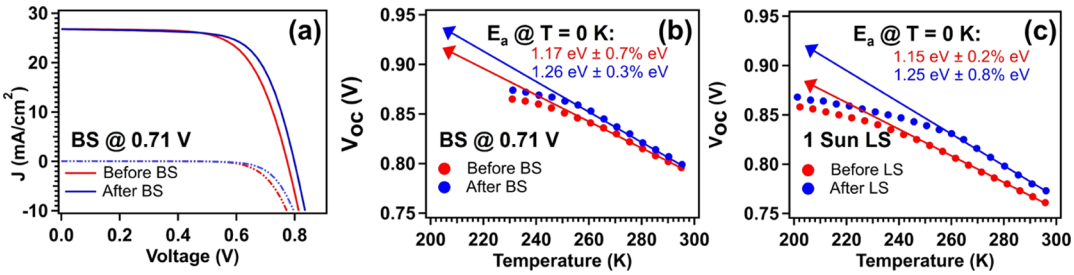

Figure 2. (a) Light (solid lines) and dark (dotted lines) $J-V$ curves before and after BS at 0.71 V, (b) V_{oc} vs T plots for a representative device before and after BS in the dark at 0.71 V, and (c) V_{oc} vs T plots for a different device before and after LS. BS and LS were both performed for 16 h at 35 °C.

depletion region. On the contrary, the device with 180 nm CdSe showed opposite behavior. Figure S3 shows the time dependence of the change in PV parameters with LS for a population of more than 30 devices with an initial 120 nm CdSe layer.

To gain more insight, we measured the performance of a separate set of 120 nm CdSe devices that were stressed only in the dark at a bias of +0.71 V for 16 h at 35 °C. This bias corresponds to the MPP for the device and produces band flattening that is close to that found near V_{oc} during illumination.[23] Both the light and dark $J-V$ curves (Figure 2a) showed an increase in the diode turn-on voltage, in good agreement with the light-soaked data for the 120 nm CdSe devices (Figure 1b,c).

The similarity in the changes observed for the light- and bias-soaked devices suggests that the origin of the change is the same in both cases. The recent work of Sankin and Krasikov,[27] and Colegrove et al.[11] suggests that the Cl and Se gradients should be established and fixed by the high-temperature $CdCl_2$ treatment (400 °C for 30 min). While the Cl and Se gradients will depend on the initial CdSe thickness, only Cu is expected to have sufficient diffusivity to migrate substantially at the relatively low temperatures examined here. Thus, a possible explanation is that Cu ion migration is responding to the change in the internal electric field. In fact, these results may have been expected from previous simulations and experimental studies of Cu ion movement in CdS/CdTe devices.[22,23] Development of a roll-over and light/dark crossover in the $J-V$ curve for all CdSe thicknesses (Figure S4) is consistent with the previous report for CdS/CdTe devices in which Cu redistribution away from the back contact was proposed.[14]

To probe how the carrier recombination may have been affected by copper redistribution, V_{oc} versus temperature data were acquired for both light-soaked and bias-soaked devices. V_{oc} vs T is a robust method for evaluating the activation energy (E_a) for the recombination mechanism that controls V_{oc} in the PV device. E_a is determined by extrapolating to zero temperature a linear fit to the data over a reasonable temperature range before carrier freeze-out occurs, for example, 250–300 K.[28−31] Figure 2b,c shows the V_{oc} vs T data before and after bias soaking (BS) and LS, respectively. Before soaking, the measured E_a values were found to be 1.17 ± 0.7 and 1.15 ± 0.2% eV by linear least-squares regression for two separate devices. After BS and LS, the E_a values were increased to 1.26 ± 0.3 and 1.25 ± 0.8% eV, respectively. The E_a values before soaking are nearly identical within the uncertainty of the measurements, as are the values determined afterward. The relatively low value for E_a prior to soaking is consistent with a dominant recombination mechanism occurring through active defects near the front of the device.[28,31] After soaking, the E_a values increased, as expected for a reduction in the carrier recombination near the front interface, in agreement with the $J-V$ data for the light- and bias-soaked samples. It is possible that the measured E_a did not increase further to the band gap value (vide infra) due to either remaining recombination near the front of the device or the on-set of bulk recombination control through either Shockley–Read–Hall or grain boundary mechanisms.

$C-V$ data also support the general conclusion that the observed changes can be explained by Cu redistribution. The Mott–Schottky plot (Figure S5) showed a larger built-in potential after LS, consistent with defect passivation. The N_A versus depletion width (W) plot showed the typical U-shaped curve (Figure 3) with nonidealities associated with factors such as a back barrier, deep levels, nonuniform carrier density, depletion of the absorber, and so forth.[14,32−34] The left branch of the N_A versus W plot is interpreted as a result of voltage sharing between the device depletion region and the back contact diode, effectively lowering the total capacitance and leading to an apparent increase in the carrier concentration.[33,35] In fully depleted devices, the right branch of the profile can show a sharp rise and the depletion width can be close to the physical thickness of the film; however, in Cu contacted devices, the onset of the right branch happens at lower values of W and the rise is shallow as seen in Figure 3.[14,34] In the present case, the right branch shows an early onset after light soak which is a signature of back diode development and has been termed "early punch-through."[33] This implies expansion of the depletion region at the back contact due to LS, as expected for copper movement away

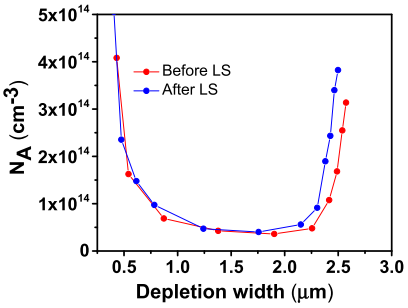

Figure 3. Carrier concentration profile of a representative CdSe/CdTe device with an initial 120 nm thick CdSe layer before and after LS.

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ACS Appl. Mater. Interfaces XXXX, XXX, XXX−XXX

from the back contact region, consistent with the development of rollover in the forward bias current (Figure S4).

In order to determine if the changes were due to filling of shallow or deep traps, the light-soaked samples were kept in the dark for 36 h and remeasured. The obtained $J-V$ curves (Figure S6) were similar to the light-soaked curves except for a small reduction in FF, suggesting long term stability, and that the modified traps are fairly deep in the band gap.[20,22]

To understand the changes occurring near the front interface in more detail, PL spectra were measured through the glass side of the devices before and after LS (Figure 4a,b).

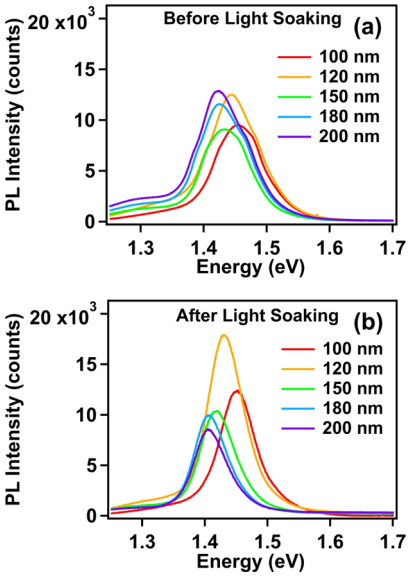

Figure 4. Room-temperature PL spectra of devices with initial CdSe layer thickness ranging from 100 to 200 nm. (a) Before LS and (b) after LS.

PL spectra for CdSe/CdTe devices have been rarely reported in the literature,[9] and data as a function of the initial CdSe layer thickness have not appeared to date. Before LS, the PL emission was relatively broad and comprised of multiple underlying emission peaks that are difficult to resolve at room temperature. The $1/e$ penetration depth of the 532 nm light used to excite the PL is about 125 nm, and thus it can be assumed that the detected PL is from the front interface region. The wavelength of the emission peak moved to lower energy as the thickness of the CdSe film was increased, as expected for a higher Se content in the graded CST layer. After LS, the emission peaks retained their order in energy but became sharper, indicating a reduction in the polydispersity of the related energetics. Interestingly, the emission from devices with 100 and 120 nm CdSe films became more intense with LS, while the emission from the samples with thicker CdSe films was unchanged or reduced. In particular, the emission peak from the 120 nm CdSe device increased in intensity by ~50% with LS.

Additional structure in the PL spectra could be discerned at 10 K. Figure 5 shows the data from the sample with a 120 nm thick CdSe layer under several conditions. The emission spectrum from the as-deposited CdSe/CdTe stack showed a weak, broad emission spanning from 1.0 to 1.5 eV (Figure S7a), consistent with the highly defective material. Weak defect-related emission has been reported on extensively for pure CdTe and is evidently present in these samples, as

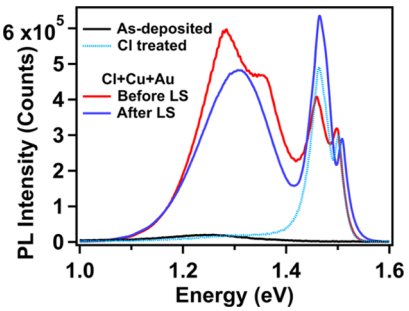

Figure 5. PL spectra at 10 K for sample fabricated with an initial CdSe thickness of 120 nm; as-deposited, after $CdCl_2$ annealing, after doping with Cu and completing the cell fabrication with Au contact, and after LS for 16 h at 35 °C.

well.[16,36−39] For pure CdTe, the defects are highly dependent on the deposition method and the degree of crystallinity, as well as the stoichiometry.[40,41] One can expect similar behavior here, with the understanding that the introduction of a graded CST layer introduces further polydispersity in the possible defects and a shifting of the emission to lower energy. From the position of the peak in the room-temperature data (Figure 4), the band gap of the emitting slab in the graded front interface region of the 120 nm CdSe device can be estimated to be ~1.44 eV, which corresponds to $x = 0.20$ in the CST layer.[42]

After $CdCl_2$ treatment, a very intense emission peak emerges near the band-edge at 10 K (Figure 5). The emission is comprised of three subpeaks at 1.464, 1.468, and 1.503 eV (see Figure S7b), similar to features observed in CdTe previously.[43,44] In $CdCl_2$-treated CSS-grown CdTe, low-temperature PL (5 to 25 K) shows near-band gap emission bands at ~1.59 eV and at 1.552 and 1.559 eV (the so-called double peak).[44] The spectral features we observe for $x = 0.2$ largely mimic the observed CdTe spectrum in this region, albeit down-shifted in energy due to the reduced band gap. We therefore tentatively assign the peaks to the following transitions: (1.503 eV) acceptor-bound exciton, (1.468 eV) free-to-bound transition, and (1.464 eV) DAP transition. Clearly, additional high-resolution studies are needed to fully resolve and assign these peaks and their energetic orders to specific transition origins for the case of CST. A schematic of the transitions is depicted in Figure S8.

Shrestha et al. measured the PL at 15 K from $CdCl_2$-treated CST alloy samples prepared by cosputtering with $x = 0.14$ and 0.21.[45] The spectra were dominated by broad, strong defect-related emission peaks at 1.294 and 1.203 eV for the $x = 0.14$ and $x = 0.21$ samples, which were assigned to free-to-bound and DAP transitions, respectively.[45,46] These peaks are not strongly present in our measurements. Shrestha et al. also observed weak emission for the two compositions at 1.452 and 1.448 eV, respectively, which were assigned to band-to-band recombination. The position of these peaks corresponds well to the band-edge peaks we report, although the underlying subpeak structure was not evident in their cosputtered samples. The stronger, more structured band-edge PL reported here, coupled with much weaker defect-related emission, is consistent with a higher degree of crystallinity and relaxation expected for samples prepared by high-temperature CSS deposition. The PL data for $CdCl_2$- and $CuCl_2$-treated samples prepared with an initial CdSe layer thickness of 180 nm showed similar results, although both the defect and band-edge

https://doi.org/10.1021/acsami.1c23937
ACS Appl. Mater. Interfaces XXXX, XXX, XXX−XXX

emissions were shifted to lower energy, as expected for a higher Se content (Figure S9a).

When the stack was doped with Cu, the emission near the band-edge was partially quenched and the broad defect-related emission at lower energy became much more intense. The broad band has an apparent primary peak at 1.28 eV and a secondary shoulder at 1.35 eV, but a more detailed peak fitting reveals three broad peaks at 1.279, 1.296, and 1.364 eV with FWHM values of 58, 169, and 51 meV, respectively (Figure S7c). Because of the breadth of these peaks and the variation of the stoichiometry in the near-surface region of the device, it is difficult to assign physical meaning to their origin. The emission may be related to the so-called Z and Z′ bands seen in pure CdTe[46] which have been ascribed to free-to-bound recombination near dislocations and DAP transitions within dislocation cores, but the addition of Cu has been reported to increase the intensity of the band-edge emission relative to these defect-related peaks[47] in contrast to what is observed here.

Clearly, further complexity arises relative to pure CdTe due to the graded Se content in the near front-surface region and the host of point defects and defect complexes that may be expected.[24,27] Though significantly more work remains to understand these effects in detail, we tentatively explain the observations by considering that an accumulation of Cu_{Cd}^{-} ionized acceptors coupled with a depletion of compensating donors in the interface region could create a spike in the p-type doping.[27] In this case, the depletion region would be less pronounced, and with the Fermi level being closer to the valance band, some defects near the front interface would remain unoccupied by electrons and could provide for more intense subband gap radiative emission. Figure 5 also shows the PL data after LS. The primary peak and shoulder were merged, and the overall emission intensity from 1.2 to 1.4 eV was reduced, while the intensity of the emission near the band-edge was substantially increased. This is likely due to changes in the atomic configurations and the degrees of association or dissociation of point defects. Following the earlier discussion, the changes in the PL spectrum should be understood in the context of an increase in the local equilibrium concentration of Cu_i^{+} species due to enhanced migration with flattened bands. Here, we can speculate that Cu_{Cd}^{-} acceptor species interact with the additional Cu_i^{+} species in the depletion region to form the neutral Cu_i−Cu_{Cd} complex.[24,27] In the presence of Se, the ionization level of the Cu_{Cd}^{-} acceptor has been predicted to be deeper in the band gap, which could change the defect into a more active recombination site.[27] In this scenario, formation of the Cu_i−Cu_{Cd} complex would reduce the radiative pathway associated with the Cu_{Cd}^{-} defect states and channel more luminescence intensity through the band-edge processes, consistent with expectations based on the observed increase in V_{oc}.

For comparison, it is interesting to consider the low-temperature PL data from the device fabricated with the 180 nm CdSe layer, which did not show improvement with LS (see discussions of Figures 1b and S2). PL measured at 10 K for the sample after Cl and Cu treatment showed broad defect emission (Figure S9a). In addition to being shifted to lower energy, as expected for the higher Se content, the band-edge emission was somewhat more intense than in the 120 nm data, while the defect-related emission was less intense. Notably, the broad defect related emission was structureless. After LS, both the broad defect-related sub-band gap emission and band-edge emission were decreased in intensity, and there was no evidence of point defect or complex modification or reorganization. Rather than restructuring of the radiative pathways, a uniform reduction of PL intensity was observed (Figure S9b). Here, the results may be understood by considering that the higher Se content may have reduced the effects of Cu migration, consistent with recent SIMS analysis.[48]

CONCLUSIONS

We performed a detailed investigation of the effect of LS on the performance of CST/CdTe PV devices as a function of the initial thickness of the CdSe layer. An increase in open-circuit voltage and a substantial increase in the efficiency were observed with LS when the CdSe layer was 120 nm thick. Companion $J-V$ data from devices that were bias-soaked in the dark and $C-V$ results obtained after devices were light-soaked suggest that copper reorganization was responsible for the observed changes. The activation energy for the dominant recombination mechanism measured by V_{oc} versus T analysis increased with both LS and BS, consistent with reduced recombination near the front interface. Room-temperature PL data collected after LS showed sharper emission bands, indicating reduced polydispersity of the emission centers. Low-temperature PL data showed reduced emission in the 1.2 to 1.4 eV defect region after LS and increase in emission at the band edge. The observed behavior is attributed to the change in the equilibrium concentration of active defects due to the migration of copper species toward the front interface. The reduction in the defect-related PL emission and the increase in the V_{oc} are explained by considering an increase in the formation of neutral Cu_i−Cu_{Cd} complex near the front interface.

MATERIALS AND METHODS

Device Fabrication. The CdSe/CdTe devices were fabricated on fluorine-doped SnO_2-coated glass substrates with an additional 50 nm intrinsic SnO_2 layer (TEC 12D; Pilkington USA). The TEC12D glass substrates were cleaned with Micro-90 detergent prior to CdSe deposition. The CdSe layer was prepared by sputtering at room temperature with an RF power of 0.1 W/cm^2 in 10 mTorr of Ar gas flowing at 23 sccm. The thickness was controlled by adjusting the deposition time, and thickness mapping was performed with spectroscopic ellipsometry to verify the thickness and spatial uniformity of the deposited CdSe films. The 3.5 μm CdTe layer was deposited by CSS with a source temperature of 560 °C and a substrate temperature of 490 °C. The base vacuum in the CSS system was ∼1 × 10^{-5} Torr prior to turning on the heating lamps. The devices were activated by dropping 100 μL of saturated $CdCl_2$-methanol solution on a 1.5″ × 1.5″ sample, drying under nitrogen, and immediately heating in dry air at 400 °C for 30 min. Copper doping was done by dipping samples in a 0.1 mM $CuCl_2$ solution in deionized water for 2 min and heating to 200 °C for 20 min in air, as previously described.[49] Devices were completed by evaporating 45 nm of Au and defining cells with an active area of 0.08 cm^2 by laser scribing. A schematic of the device structure, a cross-sectional STEM image, and a line scan of the Se profile in a 120 nm CdSe sample are shown in Figure S10.

Experiments and Data Collection. For LS, the samples were exposed to 100 mW/cm^2 incident power from an Hg vapor lamp (MVR1000). The device temperature was maintained at 35 °C throughout for both BS and LS experiments. Each experiment was done with a separate set of samples. When the samples were not being tested or stressed, they were kept at room temperature (∼21 °C) in the dark. The first $J-V$ test was done immediately after the back contact deposition (∼5 min). There was a delay of ∼3 min between

https://doi.org/10.1021/acsami.1c23937
ACS Appl. Mater. Interfaces XXXX, XXX, XXX−XXX

$J-V$ measurement and placement of the sample under light- or bias-soak. After LS, there was a delay of ∼2 min prior to the next $J-V$ test, which was sufficient for the device temperature to return to room temperature for measurement. For long-term testing, such as the data shown in Figure S3, each sample was immediately returned to the soak condition (∼1 min).

$J-V$ characteristics were measured under simulated AM1.5G illumination (exposure duration ∼ 3 s) at room temperature using a Keithley 2440 digital source meter and a LED solar simulator (MiniSol model LSH-7320) received from Newport. A calibrated silicon solar cell obtained from PV Measurements, Inc. was used to adjust the incident power to 100 mW/cm^2.

For the low-temperature V_{oc} measurements, the devices were mounted in a helium cryostat, and the temperature was varied from 300 to 200 K. Data were collected using a Keithley 2400 source-meter and a Keithley 7001 switch which is controlled by LabVIEW. C−V measurements were performed in the dark at room temperature with an AC modulating voltage of 45 mV applied at 10 kHz frequency. The DC bias voltage was swept from −3 to 1 V. Room-temperature and low-temperature steady-state PL measurements were performed with a cw 532 nm laser operating at 3.3 and 27 mW/cm^2, respectively, and the excitation was through the glass side. For high-resolution cross-sectional images, sample specimens were prepared by lifting out a lamella from a completed device by a FEI QUANTA 3D FEG instrument. Scanning transmission electron microscopy (STEM) images and line-scan energy-dispersive X-ray spectroscopy (EDXS) were performed with a Hitachi HD-2300 scanning transmission electron microscope. The cross-sectional image and the EDXS line-scanning spectra are shown in Figure S10.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsami.1c23937.

Separate plots of device parameters (V_{oc}, J_{sc}, FF, and efficiency) versus initial CdSe film thickness; plots of device parameters versus LS duration; $J-V$ plots of devices before and after LS for all CdSe film thicknesses; Mott−Schottky plot for the 120 nm CdSe device before and after LS; $J-V$ curve for device after resting in the dark; low-temperature (10 K) PL spectra recorded at different stages of device fabrication for 120 nm CdSe sample; schematic diagram of radiative transitions; low-temperature (10 K) PL spectra for the 180 nm CdSe device before and after LS; and schematic of the device structure with the STEM image and EDXS line scans for different elements (PDF)

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Notes

The authors declare no competing financial interest.

■ ACKNOWLEDGMENTS

This report is based on research sponsored by the U.S. DOE's Office of Energy Efficiency and Renewable Energy (EERE) under Solar Energy Technologies Office (SETO) Agreement DE-EE0008974 and Air Force Research Laboratory under agreement numbers FA9453-18-2-0037, FA9453-21-C-0056, and FA9453-19-C-1002. Approved for public release, distribution is unlimited. Public Affairs release approval is #AFRL-2022-1589. The U.S. Government is authorized to reproduce and distribute reprints for Governmental purposes not withstanding any copyright notation thereon. The views and conclusions contained herein are those of the authors and should not be interpreted as necessarily representing the official policies or endorsements, either expressed or implied, of Air Force Research Laboratory or the U.S. Government.

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